

MEMORY

CMOS

8 x 256K x 32 BIT, FCRAM™ CORE BASED DOUBLE DATA RATE SDRAM

MB81P643287-50/-60

CMOS 8-BANK x 262,144-WORD x 32 BIT, FCRAM Core Based
Synchronous Dynamic Random Access Memory
with Double Data Rate

■ DESCRIPTION

The Fujitsu MB81P643287 is a CMOS Synchronous Dynamic Random Access Memory (SDRAM) with Fujitsu advanced FCRAM (Fast Cycle Random Access Memory) Core Technology, containing 67,108,864 memory cells accessible in an 32-bit format. The MB81P643287 features a fully synchronous operation referenced to clock edge whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence. The MB81P643287 is designed to reduce the complexity of using a standard dynamic RAM (DRAM) which requires many control signal timing constraints. The MB81P643287 uses Double Data Rate (DDR) where data bandwidth is twice of fast speed compared with regular SDRAMs.

The MB81P643287 is ideally suited for Digital Visual Systems, High Performance Graphic Adapters, Hardware Accelerators, Buffers, and other applications where large memory density and high effective bandwidth are required and where a simple interface is needed.

The MB81P643287 adopts new I/O interface circuitry, SSTL_2 interface, which is capable of extremely fast data transfer of quality under either terminated or point to point bus environment.

■ PRODUCT LINE

Parameter		MB81P643287	
		-50	-60
Clock Frequency	CL = 3	200 MHz Max.	167 MHz Max.
	CL = 2	133 MHz Max.	111 MHz Max.
Burst Mode Cycle Time	CL = 3	2.5 ns Min.	3.0 ns Min.
	CL = 2	3.75 ns Min.	4.5 ns Min.
Random Address Cycle Time		30 ns Min.	36 ns Min.
DQS Access Time From Clock		$0.1 \times t_{CK} + 0.2$ ns Max.	$0.1 \times t_{CK} + 0.2$ ns Max.
Operating Current		460 mA Max.	405 mA Max.
Power Down Current		35 mA Max.	

Note: FCRAM is a trademark of Fujitsu Limited, Japan.

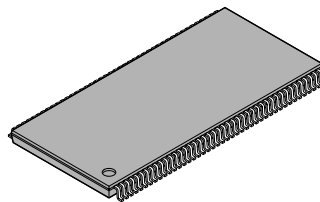
MB81P643287-50/-60

■ FEATURES

- Double Data Rate
- Bi-directional Data Strobe Signal
- Eight bank operation
- Burst read/write operation
- Programmable burst length and CAS latency
- Byte write control by DM₀ to DM₃
- Standby Power Down Mode
- 4096 Auto-refresh cycles in 32 ms
- SSTL_2 (class 2) for all signals
- V_{DD}: +2.5V Supply ± 0.2V tolerance
- V_{DDQ}: +2.5V Supply ± 0.2V tolerance

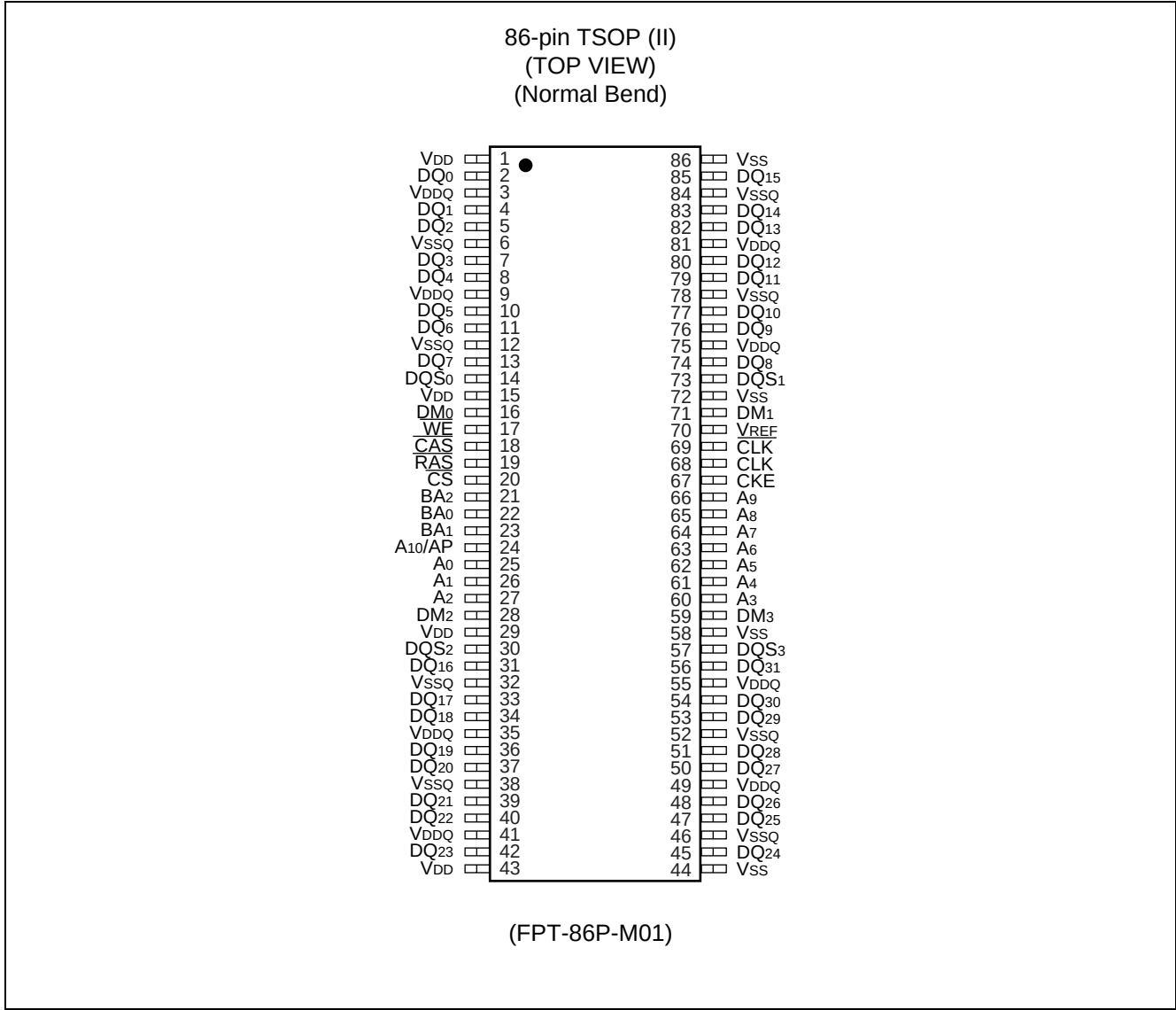
■ PACKAGE

86-pin plastic TSOP(II)



(FPT-86P-M01)
(Normal Bend)

■ PIN ASSIGNMENTS

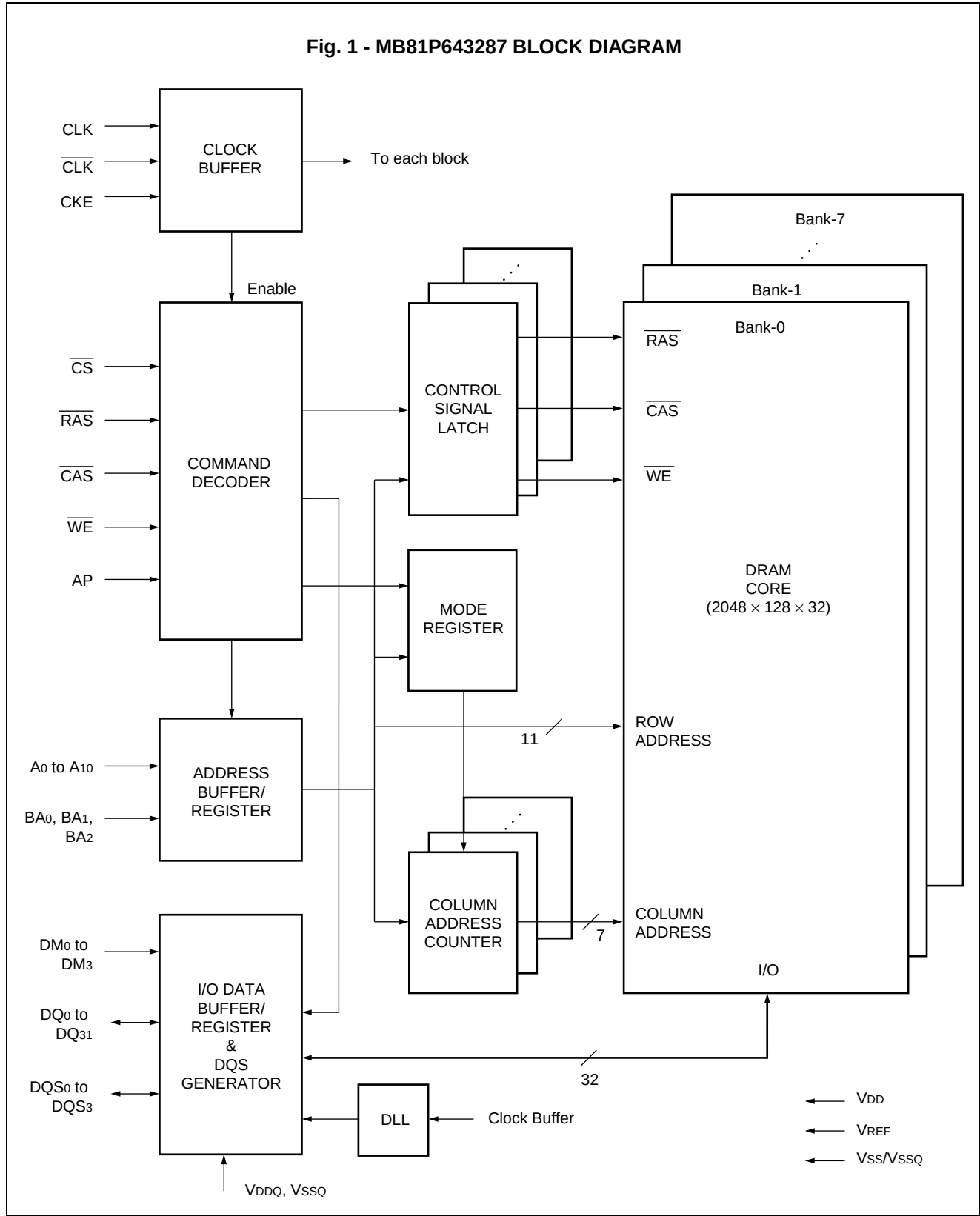


MB81P643287-50/-60

■ DESCRIPTIONS

Pin Number	Symbol	Function
1, 3, 9, 15, 29, 35, 41, 43, 49, 55, 75, 81	V_{DD}, V_{DDQ}	Supply Voltage
6, 12, 32, 38, 44, 46, 52, 58, 72, 78, 84, 86	V_{SS}, V_{SSQ}	Ground
2, 4, 5, 7, 8, 10, 11, 13, 31, 33, 34, 36, 37, 39, 40, 42, 45, 47, 48, 50, 51, 53, 54, 56, 74, 76, 77, 79, 80, 82, 83, 85	DQ_0 to DQ_{31}	Data I/O • Byte 0: DQ_0 to DQ_7 • Byte 1: DQ_8 to DQ_{15} • Byte 2: DQ_{16} to DQ_{23} • Byte 3: DQ_{24} to DQ_{31}
14, 30, 57, 73	DQS_0 to DQS_3	Data Strobe • DQS_0: for DQ_0 to DQ_7 • DQS_1: for DQ_8 to DQ_{15} • DQS_2: for DQ_{16} to DQ_{23} • DQS_3: for DQ_{24} to DQ_{31}
16, 28, 59, 71	DM_0 to DM_3	Input Mask
17	$\overline{WE}$	Write Enable
18	$\overline{CAS}$	Column Address Strobe
19	$\overline{RAS}$	Row Address Strobe
20	$\overline{CS}$	Chip Select
21, 22, 23	BA_2, BA_1, BA_0	Bank Select (Bank Address)
24	AP	Auto Precharge Enable
24, 25, 26, 27, 60, 61, 62, 63, 64, 65, 66	A_0 to A_{10}	Address Input • Row: A_0 to A_{10} • Column: A_0 to A_6
67	CKE	Power Down
68	CLK	Clock Input
69	$\overline{CLK}$	Clock Input
70	V_{REF}	Input Reference Voltage

■ BLOCK DIAGRAM



MB81P643287-50/-60

■ FUNCTION TRUTH TABLE (Note*1)

COMMAND TRUTH TABLE (Note *2, and *3)

Function	Notes	Symbol	CKE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA ₂₋₀	A _{10/AP}	A ₉₋₇	A ₆₋₀
Device Deselect	*4	DESL	H	H	X	X	X	X	X	X	X
No Operation	*4	NOP	H	L	H	H	H	X	X	X	X
Burst Stop	*5	BST	H	L	H	H	L	X	X	X	X
Read	*6	READ	H	L	H	L	H	V	L	X	V
Read with Auto-precharge	*6	READA	H	L	H	L	H	V	H	X	V
Write	*6	WRIT	H	L	H	L	L	V	L	X	V
Write with Auto-precharge	*6	WRITA	H	L	H	L	L	V	H	X	V
Bank Active ($\overline{RAS}$)	*7	ACTV	H	L	L	H	H	V	V	V	V
Precharge Single Bank	*8	PRE	H	L	L	H	L	V	L	X	X
Precharge All Banks	*8	PALL	H	L	L	H	L	V	H	X	X
Mode Register Set/ Extended Mode Register Set	*8,9,10	MRS/ EMRS	H	L	L	L	L	V	L	V	V

Notes: *1. V = Valid, L = Logic Low, H = Logic High, X = either L or H, Hi-Z = High Impedance.

*2. All commands are assumed to be valid state transitions.

*3. All inputs for command are latched on the rising edge of clock(CLK).

*4. NOP and DESL commands have the same effect on the part.

Unless specifically noted, NOP will represent both NOP and DESL command in later descriptions.

*5. BST is effective after READ command is issued.

*6. READ, READA, WRIT and WRITA commands should only be issued after the corresponding bank has been activated (ACTV command). Refer to "■ STATE DIAGRAM".

*7. ACTV command should only be issued after corresponding bank has been page closed by PRE or PALL command.

*8. Either PRE or PALL command and MRS or EMRS command are required after power up.

*9. MRS or EMRS command should only be issued after all banks have been page closed (PRE or PALL command), and DQs are in Hi-Z. Refer to "■ STATE DIAGRAM".

*10. Refer to "■ MODE REGISTER TABLE".

DM TRUTH TABLE (Effective during Write mode)

Function	Command	CKE		DM ₀	DM ₁	DM ₂	DM ₃
		(n - 1)	(n)				
Data Mask for DQ ₀ to DQ ₇	MASK0	H	X	H	X	X	X
Data Mask for DQ ₈ to DQ ₁₅	MASK1	H	X	X	H	X	X
Data Mask for DQ ₁₆ to DQ ₂₃	MASK2	H	X	X	X	H	X
Data Mask for DQ ₂₄ to DQ ₃₁	MASK3	H	X	X	X	X	H

CKE TRUTH TABLE

Current State	Function	Notes	Command	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	AP	BA ₀ to BA ₂	A ₀ to A ₁₀	DQ ₀ to DQ ₃₁
				(n-1)	(n)								
Idle	Auto-refresh	*11	REF	H	H	L	L	L	H	X	X	X	—
Idle	Self-refresh Entry	*11 *12	SELF	H	L	L	L	L	H	X	X	X	Hi-Z
Self-refresh	Self-refresh Continue		—	L	L	X	X	X	X	X	X	X	Hi-Z
Self-refresh	Self-refresh Exit		SELF	L	H	L	H	H	H	X	X	X	Hi-Z
				L	H	H	X	X	X	X	X	X	Hi-Z
Idle	Power Down Entry	*13	PDEN	H	L	L	H	H	H	X	X	X	Hi-Z
				H	L	H	X	X	X	X	X	X	Hi-Z
Power Down	Power Down Continue		—	L	L	X	X	X	X	X	X	X	Hi-Z
Power Down	Power Down Exit		PDEX	L	H	L	H	H	H	X	X	X	Hi-Z
				L	H	H	X	X	X	X	X	X	Hi-Z

*11: The REF and SELF commands should only be issued after all banks have been precharged (PRE or PALL command). In case of SELF command, it should also be issued after the last read data have been appeared on DQ. Refer to "■ STATE DIAGRAM".

*12: CKE must bring to Low level together with REF command.

*13: The PDEN command should only be issued after the last read data have been appeared on DQ and after the t_{DPL} is satisfied from last write data input.

MB81P643287-50/-60

OPERATION COMMAND TABLE (Applicable to single bank)(Note*13)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Idle	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	NOP	*15
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*16
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*16
	L	L	H	H	BA, RA	ACTV	Bank Active after I _{RCD}	
	L	L	H	L	BA, AP	PRE	NOP	
	L	L	H	L	BA, AP	PALL	NOP	*15
	L	L	L	H	X	REF/SELF	Auto-refresh or Self-refresh	*17
	L	L	L	L	MODE	MRS	Mode Register Set (Idle after I _{MRD})	*17
Bank Active	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	NOP	*15
	L	H	L	H	BA, CA, AP	READ/READA	Begin Read; Determine AP	
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Begin Write; Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	*16
	L	L	H	L	BA, AP	PRE	Precharge	
	L	L	H	L	BA, AP	PALL	Precharge	*15
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Read	H	X	X	X	X	DESL	NOP (Continue Burst to End → Bank Active)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End → Bank Active)	
	L	H	H	L	X	BST	Terminate Burst → Bank Active	
	L	H	L	H	BA, CA, AP	READ/READA	Terminate Burst, New Read; Determine AP	
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	
	L	L	H	H	BA, RA	ACTV	Illegal	*16
	L	L	H	L	BA, AP	PRE	Terminate Burst, Precharge	
	L	L	H	L	BA, AP	PALL	Terminate Burst, Precharge	*15
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Write	H	X	X	X	X	DESL	NOP (Continue Burst to End → Write Recovering)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End → Write Recovering)	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, AP	READ/READA	Terminate Burst, Start Read; Determine AP	*20
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Terminate Burst, New Write; Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	*16
	L	L	H	L	BA, AP	PRE	Terminate Burst, Precharge	*18
	L	L	H	L	BA, AP	PALL	Terminate Burst, Precharge	*15, *18
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

MB81P643287-50/-60

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Read With Auto-Precharge	H	X	X	X	X	DESL	NOP (Continue Burst to End → Precharge)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End → Precharge)	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*16
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	
	L	L	H	H	BA, RA	ACTV	Illegal	*16
	L	L	H	L	BA, AP	PRE	Illegal	*16
	L	L	H	L	BA, AP	PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Write with Auto-Precharge	H	X	X	X	X	DESL	NOP (Continue Burst to End → Write Recovering with Precharge)	
	L	H	H	H	X	NOP	NOP (Continue Burst to End → Write Recovering with Precharge)	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*16
	L	L	H	H	BA, RA	ACTV	Illegal	*16
	L	L	H	L	BA, AP	PRE	Illegal	*16
	L	L	H	L	BA, AP	PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Precharging	H	X	X	X	X	DESL	NOP (Idle after I_{RP})	
	L	H	H	H	X	NOP	NOP (Idle after I_{RP})	
	L	H	H	L	X	BST	NOP (Idle after I_{RP})	*15
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*16
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*16
	L	L	H	H	BA, RA	ACTV	Illegal	*16
	L	L	H	L	BA, AP	PRE	NOP	*16
	L	L	H	L	BA, AP	PALL	NOP	*15
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	
Bank Activating	H	X	X	X	X	DESL	NOP (Bank Active after I_{RCD})	
	L	H	H	H	X	NOP	NOP (Bank Active after I_{RCD})	
	L	H	H	L	X	BST	NOP (Bank Active after I_{RCD})	*15
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*16
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*16
	L	L	H	H	BA, RA	ACTV	Illegal	*19
	L	L	H	L	BA, AP	PRE	Illegal	*16
	L	L	H	L	BA, AP	PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
	L	L	L	L	MODE	MRS	Illegal	

MB81P643287-50/-60

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Write Recovering	H	X	X	X	X	DESL	NOP (Bank Active after I_{WRD})	
	L	H	H	H	X	NOP	NOP (Bank Active after I_{WRD})	
	L	H	H	L	X	BST	NOP (Bank Active after I_{WRD})	*15
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*16
	L	H	L	L	BA, CA, AP	WRIT/WRITA	New Write; Determine AP	
	L	L	H	H	BA, RA	ACTV	Illegal	*16
	L	L	H	L	BA, AP	PRE	Illegal	*16
	L	L	H	L	BA, AP	PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
Write Recovering with Auto-precharge	L	L	L	L	MODE	MRS	Illegal	
	H	X	X	X	X	DESL	NOP (Idle after I_{WAL})	
	L	H	H	H	X	NOP	NOP (Idle after I_{WAL})	
	L	H	H	L	X	BST	Illegal	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal	*16
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal	*16
	L	L	H	H	BA, RA	ACTV	Illegal	*16
	L	L	H	L	BA, AP	PRE	Illegal	*16
	L	L	H	L	BA, AP	PALL	Illegal	
	L	L	L	H	X	REF/SELF	Illegal	
Refreshing	L	L	L	L	MODE	MRS	Illegal	
	H	X	X	X	X	DESL	NOP (Idle after I_{RFC})	
	L	H	H	X	X	NOP/BST	NOP (Idle after I_{RFC})	
	L	H	L	X	X	READ/READA/ WRIT/WRITA	Illegal	
	L	L	H	X	X	ACTV/ PRE/PALL	Illegal	
	L	L	L	X	X	REF/SELF/ MRS	Illegal	

OPERATION COMMAND TABLE (Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function	Notes
Mode Register Setting	H	X	X	X	X	DESL	NOP (Idle after I _{MRD})	
	L	H	H	H	X	NOP	NOP (Idle after I _{MRD})	
	L	H	H	L	X	BST	Illegal	
	L	H	L	X	X	READ/READA/ WRIT/WRTA	Illegal	
	L	L	X	X	X	ACTV/PRE/ PALL/REF/ SELF/MRS	Illegal	

Abbreviations: RA = Row Address BA = Bank Address
CA = Column Address AP = Auto Precharge

- Notes: *14. All entries assume the CKE was High during the proceeding clock cycle and the current clock cycle.
 *15. Entry may affect other banks.
 *16. Illegal to bank in specified state; entry may be legal in the bank specified by BA, depending on the state of that bank.
 *17. Illegal if any bank is not idle.
 *18. Must mask preceding data that don't satisfy IDPL.
 *19. Legal if other bank specified in BA is idle state and IRRD is satisfied for that bank.
 *20. Must mask preceding data that don't satisfy IWRD.

MB81P643287-50/-60

COMMAND TRUTH TABLE FOR CKE

Current State	CKE (n-1)	CKE (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Function	Notes
Self-refresh	H	X	X	X	X	X	X	Invalid	
	L	H	H	X	X	X	X	Exit Self-refresh (Self-refresh Recovery → Idle after $t_{PDEX} + t_{SCD}$ or t_{XSNR})	
	L	H	L	H	H	H	X	Exit Self-refresh (Self-refresh Recovery → Idle after $t_{PDEX} + t_{SCD}$ or t_{XSNR})	
	L	H	L	H	H	L	X	Illegal	
	L	H	L	H	L	X	X	Illegal	
	L	H	L	L	X	X	X	Illegal	
	L	L	X	X	X	X	X	NOP (Maintain Self-refresh)	
Self-refresh Recovery	L	X	X	X	X	X	X	Invalid	
	H	H	H	X	X	X	X	Idle after t_{SCD} or t_{XSNR}	
	H	H	L	H	H	H	X	Idle after t_{SCD} or t_{XSNR}	
	H	H	L	H	H	L	X	Illegal	
	H	H	L	H	L	X	X	Illegal	
	H	H	L	L	X	X	X	Illegal	
	H	L	X	X	X	X	X	Illegal	
Power Down	H	X	X	X	X	X	X	Invalid	
	L	H	H	X	X	X	X	Power Down Exit → Return to original state after t_{PDEX}	
	L	H	L	H	H	H	X	Power Down Exit → Return to original state after t_{PDEX}	
	L	H	L	H	H	L	X	Illegal	
	L	H	L	H	L	X	X	Illegal	
	L	H	L	L	X	X	X	Illegal	
	L	L	X	X	X	X	X	NOP (Maintain Power Down Mode)	

COMMAND TRUTH TABLE FOR CKE (continued)

Current State	CKE (n-1)	CKE (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Function	Notes
All Banks Idle	H	H	H	X	X	X	X	NOP	
	H	H	L	H	X	X	V	Refer to the Command Truth Table.	
	H	H	L	L	H	X	V	Refer to the Command Truth Table.	
	H	H	L	L	L	H	X	Auto-refresh	
	H	H	L	L	L	L	V	Mode Register Set	*21
	H	L	H	X	X	X	X	Power Down Entry	*22
	H	L	L	H	H	H	X	Power Down Entry	*22
	H	L	L	H	H	L	X	Illegal	
	H	L	L	H	L	X	X	Illegal	
	H	L	L	L	H	X	X	Illegal	
	H	L	L	L	L	H	X	Self-refresh Entry	*22
	H	L	L	L	L	L	X	Illegal	
	L	X	X	X	X	X	X	Invalid	
Bank Active	H	H	X	X	X	X	X	Refer to the Command Truth Table.	
	H	L	X	X	X	X	X	Illegal	
	L	H	X	X	X	X	X	Invalid	
	L	L	X	X	X	X	X	Invalid	

MB81P643287-50/-60

COMMAND TRUTH TABLE FOR CKE (continued)

Current State	CKE (n-1)	CKE (n)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Function	Notes
Bank Activating, Read, Write, Write Recovering, Precharging	H	H	X	X	X	X	X	Refer to the Command Truth Table.	
	H	L	X	X	X	X	X	Illegal	*23
	L	H	X	X	X	X	X	Invalid	
	L	L	X	X	X	X	X	Invalid	
Any State Other Than Listed Above	L	X	X	X	X	X	X	Invalid	
	H	H	X	X	X	X	X	Refer to the Command Truth Table.	
	H	L	X	X	X	X	X	Illegal	*23
Refresh	H	L	H	L	L	L	X	Illegal	
	H	L	L	H	H	H	X	Illegal	
	H	L	L	H	H	L	X	Illegal	
	H	L	L	H	L	X	X	Illegal	
	H	L	L	L	X	X	X	Illegal	
	L	L	X	X	X	X	X	Invalid	
	L	H	X	X	X	X	X	Invalid	
	H	H	X	X	X	X	X	Refer to the Command Truth Table.	

Notes: *21. Refer to "■ MODE REGISTER TABLE".

*22. PDEN and SELF command should only be issued after the last read data have been appeared on DQ.

*23. The Clock Suspend mode is not supported on this device and it is illegal if CKE is brought to Low during the Burst Read or Write mode.

■ STATE DIAGRAM

MINIMUM CLOCK LATENCY OR DELAY TIME FOR SINGLE BANK OPERATION

Second command (same bank) First command	MRS	ACTV	READ	READA	WRIT	WRITA	BST	^{*1} PRE	PALL	REF	SELF
MRS	IMRD	IMRD					IMRD	IMRD	IMRD	IMRD	IMRD
ACTV			IRCD	^{*4} IRCD	IRCD	^{*4} IRCD	1	IRAS	IRAS		
READ			1	^{*4} 1	^{*3} LRWD	^{*3, 4} LRWD	1	^{*4} 1	^{*4} 1		
READA	^{*5, 6} BL/2 + IRP	BL/2 + IRP						^{*4} BL/2 + IRP	^{*4} BL/2 + IRP	^{*6} BL/2 + IRP	^{*5, 6} BL/2 + IRP
WRIT			^{*7} LRWD	^{*4, 7} LRWD	1	^{*4} 1		^{*4, 7} IDPL	^{*4, 7} IDPL		
WRITA	^{*6} IWAL	IWAL						^{*4} IWAL	^{*4} IWAL	^{*6} IWAL	^{*6} IWAL
BST			1	1	^{*3} IBSNC	^{*3} IBSNC	1	^{*4} 1	^{*4} 1		
PRE	^{*5, 6} IRP	IRP					1	1	^{*4} 1	^{*6} IRP	^{*5, 6} IRP
PALL	^{*5} IRPA	IRPA					1	1	1	IRPA	^{*5} IRPA
REF	IRFC	IRFC					IRFC	IRFC	IRFC	IRFC	IRFC
SELF	IXSNR	IXSNR					IXSNR	IXSNR	IXSNR	IXSNR	IXSNR

Notes: *1. $BL/2 = t_{CK} \times BL / 2$. (Example: In case of $BL = 4$, $BL/2$ means 2 clocks.)

*2. Assume PALL command does not affect any operation on the other bank(s).

*3. Assume no I/O conflict.

*4. IRAS must be satisfied.

*5. Assume all outputs are in High-Z state.

*6. Assume all other banks are in idle state.

*7. IDPL and LRWD are specified from last data input and assumed preceding pair of write data are masked by DM₀ to DM₃ input.

 Illegal Command

MB81P643287-50/-60

MINIMUM CLOCK LATENCY OR DELAY TIME FOR MULTIPLE BANK OPERATION

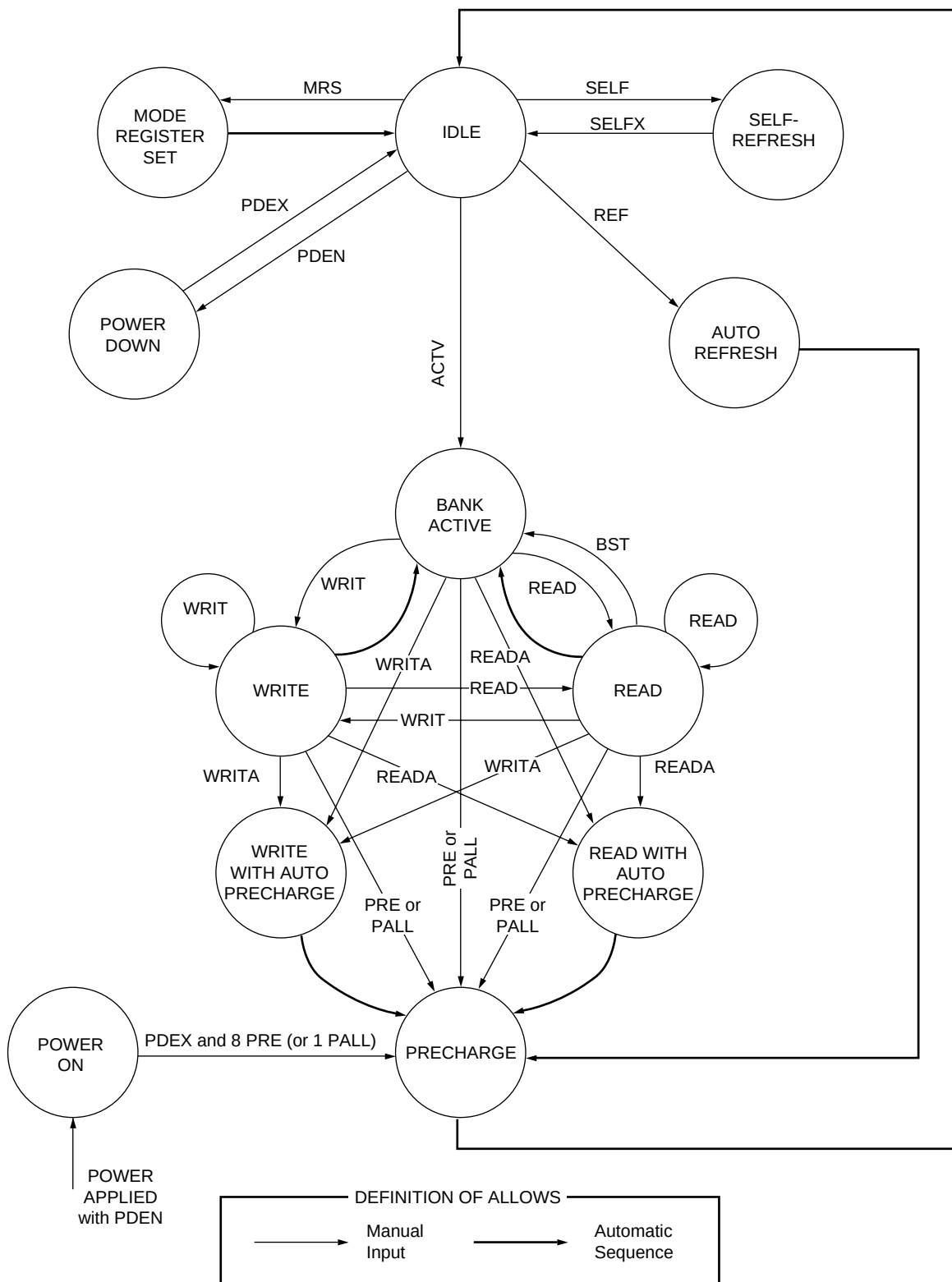
Second command (other bank) *10 First command	MRS	ACTV	*8 READ	*8 READA	*8 WRIT	*8 WRITA	*9 BST	*2, 9 PRE	PALL	REF	SELF
MRS	lMRD	lMRD					lMRD	lMRD	lMRD	lMRD	lMRD
ACTV		*6 lRRD	*11 1	*11 1	*11 1	*11 1	*11 1	1	lRAS		
READ		*6 1	1	1	*3 lRWD	*3 lRWD	1	1	*4 1		
READA	*5, 6 BL/2+ lRP	*6 1	*4 1	*4 1	*3, 4 lRWD	*3, 4 lRWD		1	BL/2+ lRP	*6 BL/2+ lRP	*5, 6 BL/2+ lRP
WRIT		*6 1	*7 lWRD	*7 lWRD	1	1		1	*4, 7 lDPL		
WRITA	*6 lWAL	*6 1	*4 BL/2 + lWRD	*4 BL/2 + lWRD	*4 1	*4 1		1	lWAL	*6 lWAL	*6 lWAL
BST		*6 1	*11 1	*11 1	*3, 11 lBSNC	*3, 11 lBSNC	1	1	*4 1		
PRE	*5, 6 lRP	*6 1	*11 1	*11 1	*3, 11 1	*3, 11 1	*11 1	1	*4 1	*6 lRP	*5, 6 lRP
PALL	*5 lRPA	lRPA					1	1	1	lRPA	*5 lRPA
REF	lRFC	lRFC					lRFC	lRFC	lRFC	lRFC	lRFC
SELF	lXSNR	lXSNR					lXSNR	lXSNR	lXSNR	lXSNR	lXSNR

- Notes:
- *1. $BL/2 = t_{CK} \times BL / 2$. (Example: In case of $BL = 4$, $BL/2$ means 2 clocks.)
 - *2. Assume PALL command does not affect any operation on the other bank(s).
 - *3. Assume no I/O conflict.
 - *4. I_{RAS} must be satisfied.
 - *5. Assume all outputs are in High-Z state.
 - *6. Assume the other bank(s) is in idle state.
 - *7. $IDPL$ and $IWRD$ are specified from last data input and assumed preceding pair of write data are masked by DM_0 to DM_3 input.
 - *8. Assume the other bank(s) is in active state and I_{RCD} is satisfied.
 - *9. Assume the other bank(s) is in active state and I_{RAS} is satisfied.
 - *10. Second command have to follow the minimum clock latency or delay time of single bank operation in other bank (second command is asserted.)
 - *11. Assume other banks are not in READA/WRITA state.



Illegal Command.

Fig. 2 - STATE DIAGRAM (Simplified for Single Bank Operation)



■ FUNCTIONAL DESCRIPTION

DDR, Double Data Rate Function

The regular SDRAM read and write cycle have only used the rising edge of external clock input. When clock signal goes to High from Low at the read mode, the read out data will be available at every rising clock edge after the specified latency up to burst length. The MB81P643287 DDR FCRAM features a twice of data transfer rate within a same clock period by transferring data at every rising and falling clock edge. Refer to Figure 3.

FCRAM™

The MB81P643287 utilizes FCRAM core technology. The FCRAM is an acronym of Fast Cycle Random Access Memory and provides very fast random cycle time, low latency and low power consumption than regular DRAMs.

CLOCK INPUT (CLK, $\overline{\text{CLK}}$)

The MB81P643287 adopts differential clock scheme. CLK is a master clock and its rising edge is used to latch all command and address inputs. $\overline{\text{CLK}}$ is a complementary clock input.

The MB81P643287 implements Delay Locked Loop (DLL) circuit. This internal DLL tracks the signal cross point between CLK and $\overline{\text{CLK}}$ and generate some clock cycle delay for the output buffer control at Read mode.

The internal DLL circuit requires some Lock-on time for the stable delay time generation. In order to stabilize the delay, a constant stable clock input for t_{PCD} period is required during the Power-up initialization and a constant stable clock input for t_{SCD} period is also required after Self-refresh exit as specified t_{SCD} prior to the any command.

POWER DOWN (CKE)

CKE is a synchronous input signal and enables power down mode.

When all banks are in idle state, CKE controls Power Down (PD) and Self-refresh mode. The PD and Self-refresh is entered when CKE is brought to Low and exited when it returns to High.

During the Power Down and Self-refresh mode, both CLK and $\overline{\text{CLK}}$ are disabled after specified time.

CKE does not have a Clock Suspend function unlike CKE pin of regular SDRAMs, and it is illegal to bring CKE into Low if any read or write operation is being performed. For the detail, refer to Timing Diagrams.

It is recommended to maintain CKE to be Low until V_{DD} gets in the specified operating range in order to assure the power-up initialization.

CHIP SELECT ($\overline{\text{CS}}$)

$\overline{\text{CS}}$ enables all commands inputs, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$, and address input. When $\overline{\text{CS}}$ is High, all command signals are negated but internal operation such as burst cycle will not be suspended.

COMMAND INPUTS ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$)

As well as regular SDRAMs, each combination of $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ input in conjunction with $\overline{\text{CS}}$ input at a rising edge of the CLK determines SDRAM operation. Refer to "■FUNCTION TRUTH TABLE".

MB81P643287-50/-60

BANK ADDRESS (BA₀ to BA₂)

The MB81P643287 has eight internal banks and each bank is organized as 256K words by 32-bit. Bank selection by BA occurs at Bank Active command (ACTV) followed by read (READ or READA), write (WRIT or WRITA), and Precharge(PRE) command.

ADDRESS INPUTS (A₀ to A₁₀)

Address input selects an arbitrary location of a total of 2,097,152 words of each memory cell matrix within each bank. A total of twenty address input signals are required to decode such a matrix. DDR SDRAM adopts an address multiplexer in order to reduce the pin count of the address line. At a Bank Active command (ACTV), eleven Row addresses are initially latched as well as three Bank addresses and the remainder of seven Column addresses are then latched by a Column address strobe command of either a read command (READ or READA) or write command (WRIT or WRITA).

DATA STROBE (DQS₀ to DQS₃)

DQS₀ to DQS₃ are bi-directional signal and represent byte 0 to byte 3, respectively. During Read operation, DQS₀ to DQS₃ provides the read data strobe signal that is intended to use input data strobe signal at the receiver circuit of the controller(s). It turns Low before first data is coming out and toggle High to Low or Low to High till end of burst read. Refer to Figure 3 for the timing example.

The CAS Latency is specified to the first Low to High transition of these DQS₀ to DQS₃ output.

During the write operation, DQS₀ to DQS₃ are used to latch write data and Data Mask signals. As well as the behavior of read data strobe, the first rising edge of DQS₀ to DQS₃ input latches first input data and following falling edge of DQS₀ to DQS₃ signal latches second input data. This sequence shall be continued till end of burst count. Therefore, DQS₀ to DQS₃ must be provided from controller that drives write data.

Note that DQS₀ to DQS₃ input signal should not be tristated from High at the end of write mode.

DATA INPUTS AND OUTPUTS (DQ₀ to DQ₃₁)

Input data is latched by DQS₀ to DQS₃ input signal and written into memory at the clock following the write command input. Output data is obtained together with DQS₀ to DQS₃ output signals at programmed read CAS latency.

The polarity of the output data is identical to that of the input. Data is valid after DQS₀ to DQS₃ output signal transitions (t_{QSQ}) as specified in Data Valid Time (t_{DV}).

WRITE DATA MASK (DM₀ to DM₃)

DM₀ to DM₃ are active High enable inputs and represent byte 0 to byte 3 respectively. DM₀ to DM₃ have a data input mask function, and are also sampled by DQS₀ to DQS₃ input signal together with input data.

During write cycle, DM₀ to DM₃ provide byte mask function. When DM_x = High is latched by a DQS₀ to DQS₃ signal edge, data input at the same edge of DQS₀ to DQS₃ is masked.

During read cycle, all DM₀ to DM₃ are inactive and do not have any effect on read operation.

Refer to DM₀ to DM₃ TRUTH TABLE.

BURST MODE OPERATION AND BURST TYPE

The burst mode provides faster memory access and MB81P643287 read and write operations are burst oriented. The burst mode is implemented by keeping the same Row address and by automatic strobing Column address in every single clock edge till programmed burst length(BL). Access time of burst mode is specified as t_{ACC} . The internal column address counter operation is determined by a mode register which defines burst type(BT) and burst count length(BL) of 2, 4 or 8 bits of boundary. In order to terminate or to move from the current burst mode to the next stage while the remaining burst count is more than 2, the following combinations will be required.

Current Stage	Next Stage	Method (Assert the following command)	
Burst Read	Burst Read	Read Command	
Burst Read	Burst Write	1st Step	Burst Stop Command (BST)
		2nd Step	Write Command after I_{BSNC}
Burst Write	Burst Write	Write Command	
Burst Write	Burst Read	1st Step	Data Mask Input
		2nd Step	Read Command after I_{WRD} from last data input
Burst Read	Precharge	Precharge Command	
Burst Write	Precharge	1st Step	Data Mask Input
		2nd Step	Precharge Command after I_{DPL} from last data input

The burst type is sequential only. The sequential mode is an incremental decoding scheme within a boundary address to be determined by count length, it assigns +1 to the previous (or initial) address until reaching the end of boundary address and then wraps round to the least significant address(= 0). If the first access of column address is even (0), the next address will be odd (1), or vice-versa.

Burst Length	Starting Column Address $A_2 \ A_1 \ A_0$	Sequential Mode
2	X X 0	0 – 1
	X X 1	1 – 0
4	X 0 0	0 – 1 – 2 – 3
	X 0 1	1 – 2 – 3 – 0
	X 1 0	2 – 3 – 0 – 1
	X 1 1	3 – 0 – 1 – 2
8	0 0 0	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7
	0 0 1	1 – 2 – 3 – 4 – 5 – 6 – 7 – 0
	0 1 0	2 – 3 – 4 – 5 – 6 – 7 – 0 – 1
	0 1 1	3 – 4 – 5 – 6 – 7 – 0 – 1 – 2
	1 0 0	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3
	1 0 1	5 – 6 – 7 – 0 – 1 – 2 – 3 – 4
	1 1 0	6 – 7 – 0 – 1 – 2 – 3 – 4 – 5
	1 1 1	7 – 0 – 1 – 2 – 3 – 4 – 5 – 6

BURST STOP COMMAND (BST)

The Burst Stop command (BST) terminates the burst read operation except for a case that Auto-precharge option is asserted. When the BST command is issued during the burst read operation, the all output buffers, DQs and DQS₀ to DQS₃, will turn to High-Z state after some latencies that to be matched with programmed CAS latency and internal bank state remains active state.

In a case of terminating the burst write operation, the BST command should not be issued at any time during burst write operation. Refer to previous page for the write interrupt and termination rule.

PRECHARGE AND PRECHARGE OPTION (PRE, PALL)

The DDR SDRAM memory core is the same as conventional DRAMs', requiring precharge and refresh operations. Precharge rewrites the bit line and to reset the internal Row address line and is executed by the precharge operation (PRE or PALL). With the precharge operation, DDR SDRAM will automatically be in standby state after specified precharge time (t_{RP} , t_{RPA}).

The precharged bank is selected by combination of AP and bank address (BA) when precharge command is issued. If AP = High, all banks are precharged regardless of BA (PALL command). If AP = Low, a bank to be selected by BA is precharged (PRE command).

The auto-precharge enters precharge mode at the end of burst mode of read or write without Precharge command issue. This auto-precharge is entered by AP = High when a Read (READ) or Write (WRIT) command is issued. Applying BST is illegal if the Auto-precharge option is used.

Refer to "FUNCTION TRUTH TABLE".

AUTO-REFRESH (REF)

Auto-refresh uses the internal refresh address counter. The MB81P643287 Auto-refresh command (REF) automatically generates Bank Active and Precharge command internally. All banks of SDRAM should be precharged prior to the Auto-refresh command. The Auto-refresh command should also be issued within every 8 μ s period.

SELF-REFRESH ENTRY (SELF)

Self-refresh function provides automatic refresh by an internal timer as well as Auto-refresh and will continue the refresh operation until cancelled by SELF_{FX}.

The Self-refresh mode is entered by applying an Auto-refresh command in conjunction with CKE = Low (SELF). Once MB81P643287 enters the self-refresh mode, all inputs except for CKE can be either logic high or low level state and outputs will be in a High-Z state. During Self-refresh mode, CKE = Low should be maintained. SELF command should only be issued after last read data has been appeared on DQ.

Note: When the burst refresh method is used, a total of 4096 auto-refresh commands within 4 ms must be asserted prior to the self-refresh mode entry.

SELF-REFRESH EXIT (SELF_{FX})

To exit Self-refresh mode, CKE must bring to High for at least 2 clock cycles together with NOP condition.

Refer to Timing Diagram for the detail procedure. It is recommended to issue at least one Auto-refresh command just after the t_{RFC} period to avoid the violation of refresh period.

WARNING: A stable clock for t_{SCD} period with a constant duty cycle must be supplied prior to applying any read command to insure the DLL is locked against the latest device conditions.

Note: When the burst refresh method is used, a total of 4096 auto-refresh commands within 4 ms must be asserted both before the self-refresh entry and after the self-refresh exit.

MODE REGISTER SET (MRS)

The mode register of SDRAM provides a variety of different operations. The register consists of four operation fields; Burst Length, Burst Type, CAS Latency, and Test Mode Entry (This Test Mode Entry must not be used). Refer to MODE REGISTER TABLE.

The mode register can be programmed by the Mode Register Set command (MRS). Each field is set by the address line. Once a mode register is programmed, the contents of the register will be held until re-programmed by another MRS command (or part loses power). MRS command should only be issued on condition that all banks are in idle state and all DQS are in High-Z. The condition of the mode register is undefined after the power-up stage. It is required to set each field at power-up initialization.

Refer to POWER-UP INITIALIZATION below.

Note: The Extended Mode Register Set command (EMRS) and its DLL Enable function of EMRS field is only used at power-on sequence.

POWER-UP INITIALIZATION

The MB81P643287 internal condition at and after power-up will be undefined. It is required to follow the following Power On Sequence to execute read or write operation.

1. Apply V_{DD} voltage to all V_{DD} pins before or at the same time as V_{DDQ} pins and attempt to maintain all input signals to be Low state (or at least CKE to be Low state).
2. Apply V_{DD} voltage to all V_{DDQ} pins before or at the same time as V_{REF} and V_{TT} .
3. Apply V_{REF} and V_{TT} . (V_{TT} is applied to the system).
4. Start clock after all power supplies reached in a specified operating range and maintain stable condition for a minimum of 200 μ s.
5. After the minimum of 200 μ s stable power and clock, apply NOP condition and take CKE to be High state.
6. Issue Precharge All Banks (PALL) command or Precharge Single Bank (PRE) command to every banks.
7. Issue EMRS to enable DLL, DE = Low.
8. Issue Mode Register Set command (MRS) to reset DLL, DR = High. An additional clock input for I_{PCD} *¹ period is required to lock the DLL.
9. Apply minimum of two Auto-refresh command (REF).^{*2}
10. Program the mode register by Mode Register Set command (MRS) with DR = Low.^{*2}

*1: The I_{PCD} depends on operating clock period. The I_{PCD} is counted from "DLL Reset" at step-8 to any command input at step-10.

*2: The Mode Register Set command (MRS) can be issued before two Auto-refresh cycle.

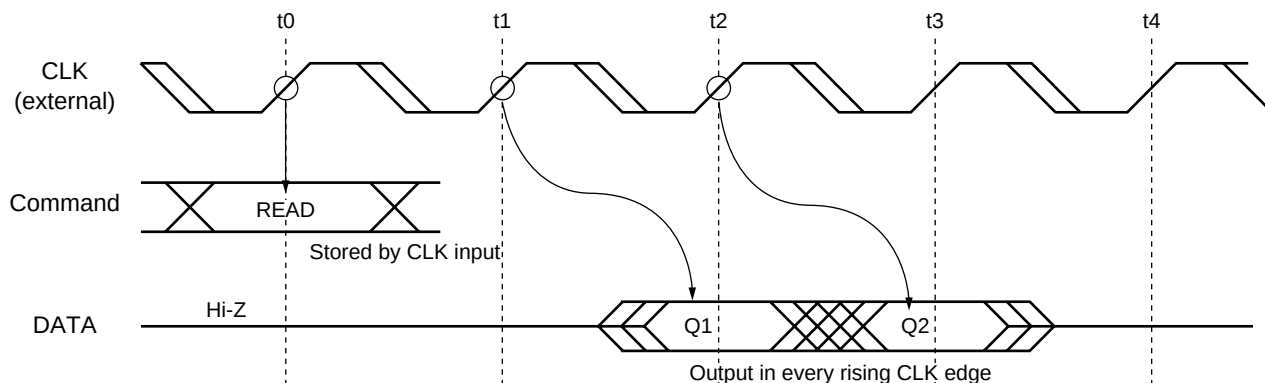
POWER-DOWN

The MB81P643287 uses multiple power supply voltage. It is required to follow the reversed sequence of above Power On Sequence.

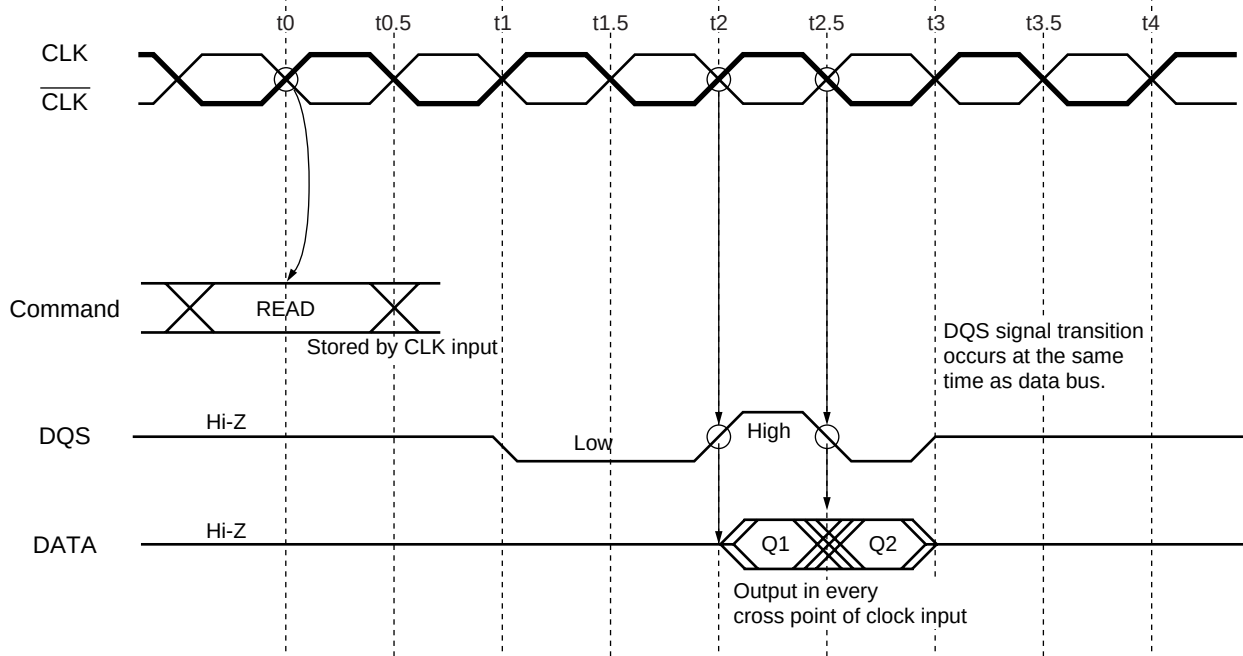
1. Take all input signals to be V_{SS} or High-Z.
2. Deapply V_{DDQ} .
3. Deapply V_{DD} at the same time as V_{DDQ} .

Fig. 3 - SDRAM READ TIMING EXAMPLE (@ CL=2 & BL=2)

<SDRAM>



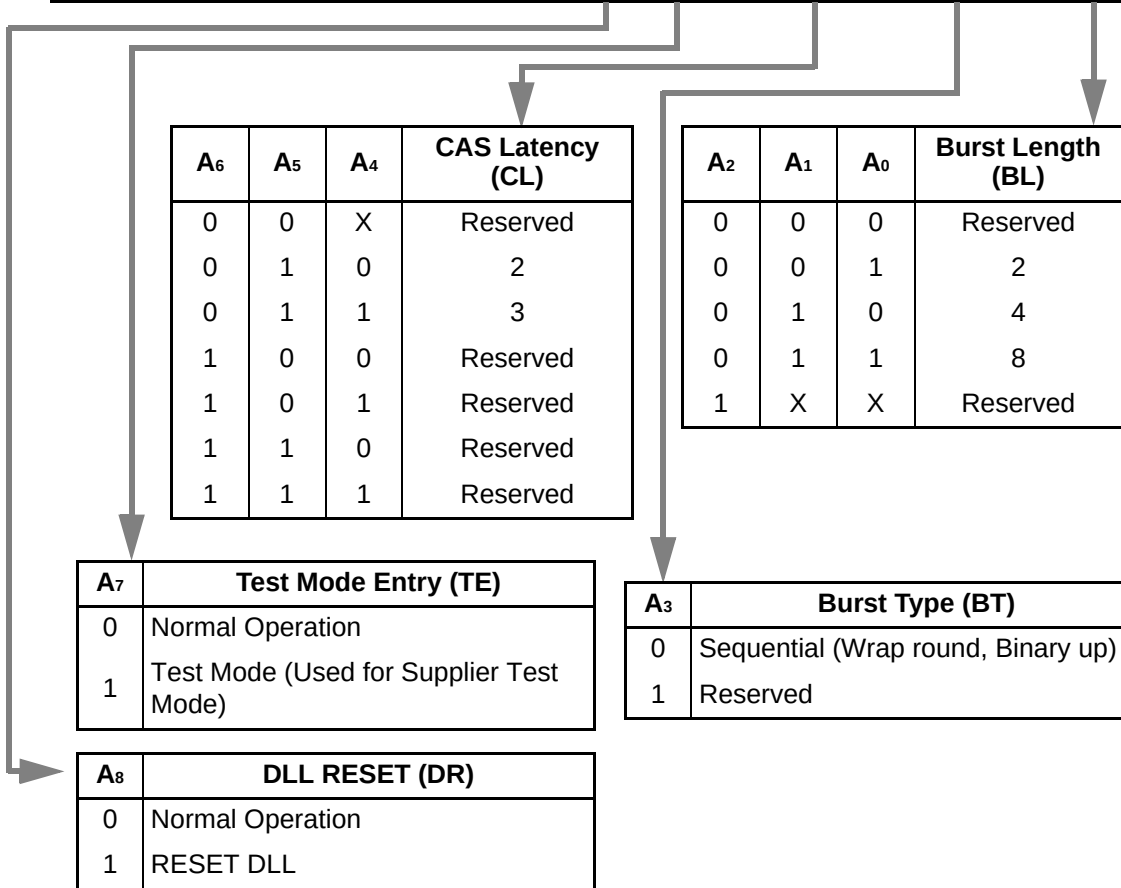
< DDR SDRAM >



MODE REGISTER TABLE

MODE REGISTER SET

ADDRESS	BA ₂	BA ₁	BA ₀	A ₁₀	A ₉	A ₈	A ₇	A ₆ to A ₄	A ₃	A ₂ to A ₀
REGISTER	0 ^{*1}	0 ^{*1}	0 ^{*1}	0	0	DR	TE	CL	BT	BL



EXTENDED MODE REGISTER SET (Note *4)

ADDRESS	BA ₂	BA ₁	BA ₀	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀
EXTENDED MODE REGISTER	0 ^{*2}	0 ^{*2}	1 ^{*2}	RESERVED ^{*3}										DE

A ₀	DLL Enable (DE)
0	DLL Enable
1	DLL Disable

*1: A combination of BA₂ = BA₁ = BA₀ = 0 (Low) selects standard Mode Register.

*2: A combination of BA₁ = BA₂ = 0 and BA₀ = 1 (High) selects Extended Mode Register.

*3: These RESERVED field in EMRS must be set as 0.

MB81P643287-50/-60

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Voltage of V_{DD} Supply Relative to V_{SS}	V_{DD} , V_{DDQ}	-0.5 to +3.6	V
Voltage at Any Pin Relative to V_{SS}	V_{IN} , V_{OUT}	-0.5 to +3.6	V
Short Circuit Output Current	I_{OUT}	± 50	mA
Power Dissipation	P_D	2.0	W
Storage Temperature	T_{STG}	-55 to +125	°C

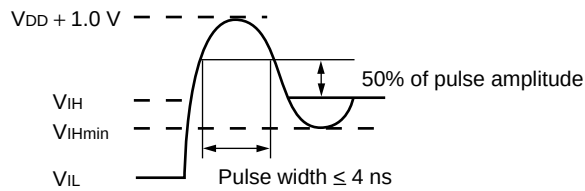
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

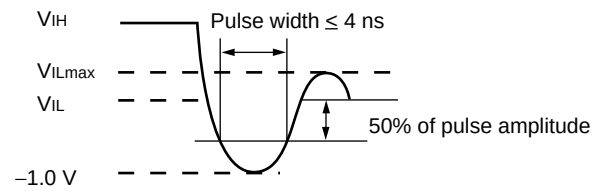
(Referenced to V_{SS})

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	2.3	2.5	2.7	V
		V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V
		V_{SS} , V_{SSQ}	0	0	0	V
Input Reference Voltage	*1	V_{REF}	$V_{DDQ} \times 0.49$	$V_{DDQ} \times 0.5$	$V_{DDQ} \times 0.51$	V
Termination Voltage	*2	V_{TT}	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
Single Ended SSTL DC Level Input High Voltage	*3	$V_{IH} (DC)$	$V_{REF} + 0.25$	—	$V_{DDQ} + 0.1$	V
Single Ended SSTL DC Level Input Low Voltage	*3	$V_{IL} (DC)$	- 0.1	—	$V_{REF} - 0.25$	V
Single Ended SSTL AC Level Input High Voltage	*3, *5	$V_{IH} (AC)$	$V_{REF} + 0.35$	—	—	V
Single Ended SSTL AC Level Input Low Voltage	*3, *5	$V_{IL} (AC)$	—	—	$V_{REF} - 0.35$	V
Differential DC Level Input Voltage Range	*3	$V_{IN} (DC)$	- 0.1	—	$V_{DDQ} + 0.1$	V
Differential DC Level Differential Input Voltage	*3	$V_{SWING} (DC)$	0.5	—	$V_{DDQ} + 0.2$	V
Differential AC Level Differential Input Voltage	*3	$V_{SWING} (AC)$	0.7	—	—	V
Differential AC Level Input Crosspoint Voltage	*3	$V_X (AC)$	$V_{DDQ}/2 - 0.2$	$V_{DDQ}/2$	$V_{DDQ}/2 + 0.2$	V
Differential Input Signal Offset Voltage	*4	$V_{ISO} (AC)$	$V_{DDQ}/2 - 0.2$	$V_{DDQ}/2$	$V_{DDQ}/2 + 0.2$	V
Termination Resistor (SSTL I/Os)	*2	R_T	—	50	—	Ω
Ambient Temperature		T_A	0	—	70	°C

Note 5.



Note 6.



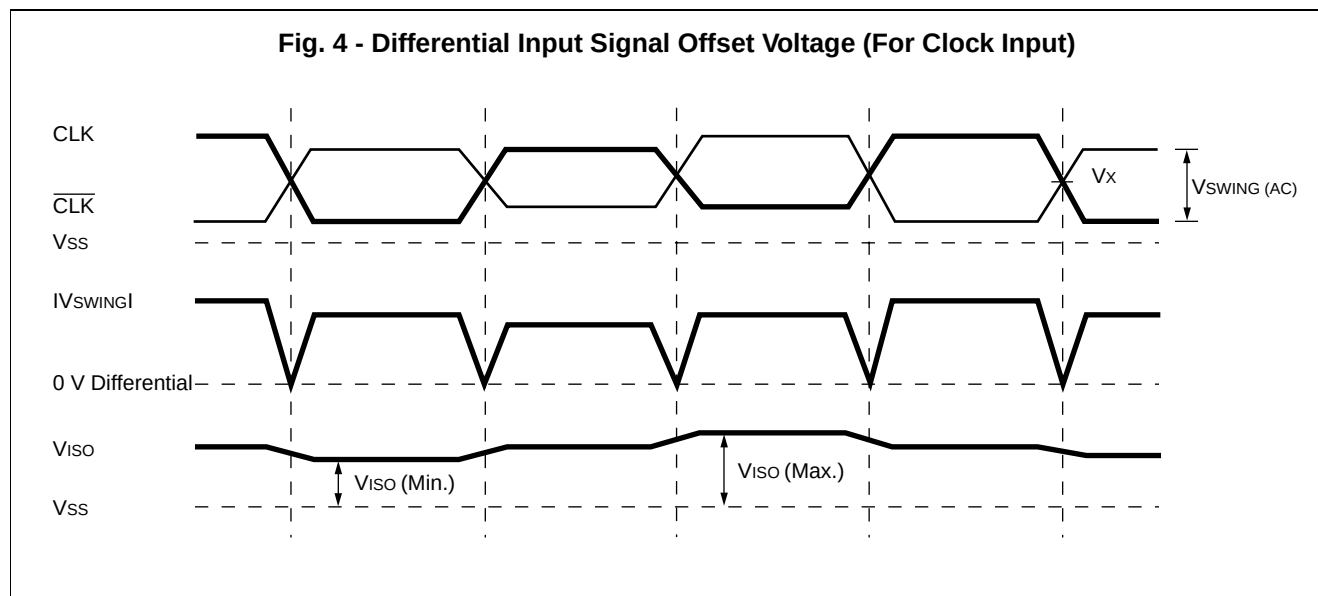
- Notes:
- *1. V_{REF} is expected to track variations in the DC level of V_{DDQ} of the transmitting device. Peak-to-Peak noise level on V_{REF} may not exceed $\pm 2\%$ of the supplied DC value.
 - *2. V_{TT} is used for SSTL_2 bus and is not applied to the device. V_{TT} is expected to be set equal to V_{REF} and must be track variations in the DC level of V_{REF} .
 - *3. Applicable when signal(s) is terminated to the V_{TT} of SSTL_2 bus.
 - *4. V_{ISO} means $\{V_{IN(CLK)} + V_{IN(\overline{CLK})}\} / 2$. Refer to Differential Input Signal Definition.
 - *5. Overshoot limit: $V_{IH} (Max.) = V_{DD} + 1.0V$ for pulse width ≤ 4 ns acceptable, pulse width measured at 50% of pulse amplitude.
 - *6. Undershoot limit: $V_{IL} (Min.) = V_{SS} - 1.0V$ for pulse width ≤ 4 ns acceptable, pulse width measured at 50% of pulse amplitude.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

Differential Input Signal Definition



■ CAPACITANCE

($T_A = 25^\circ C$, $f = 1$ MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance, Address & Control	C_{IN1}	2.5	—	3.5	pF
Input Capacitance, CLK & $\overline{CLK}$	C_{IN2}	2.5	—	3.5	pF
Input Capacitance, DM ₀ to DM ₃	C_{IN3}	4.0	—	5.5	pF
I/O Capacitance	$C_{I/O}$	4.0	—	5.5	pF

MB81P643287-50/-60

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Note *1,*2,*3

Parameter		Symbol	Condition	Value		Unit
				Min.	Max.	
Output Minimum Source DC Current		$I_{OH(DC)}$	$V_{DDQ} = 2.3V$, $V_{OH} = V_{DDQ} - 0.43V$	-15.2	—	mA
Output Minimum Sink DC Current		$I_{OL(DC)}$	$V_{DDQ} = 2.3V$, $V_{OL} = +0.35V$	15.2	—	mA
Input Leakage Current (any input)		I_{LI}	$0V \leq V_{IN} \leq V_{DD}$; All other pins not under test = 0 V	-10	10	μA
Output Leakage Current		I_{LO}	$0V \leq V_{IN} \leq V_{DD}$; Data out disabled	-10	10	μA
V_{REF} Current		I_{REF}		-10	10	μA
Operating Current (Average Power Supply Current)	MB81P643287-50	I_{DD1S}	Burst Length = 2 $t_{CK} = \text{Min.}$, One bank active, Address change up to 3 times during I_{RC} (Min.) $0V \leq V_{IN} \leq V_{IL}$ (Max.), V_{IH} (Min.) $\leq V_{IN} \leq V_{DD}$	—	460	mA
	MB81P643287-60				405	
Standby Current	MB81P643287-50	I_{DD2N}	CKE = V_{IH} , $t_{CK} = \text{Min.}$ All banks idle, NOP commands only, Input signals (except to CMD) are changed one time during 20 ns $0V \leq V_{IN} \leq V_{IL}$ (Max.), V_{IH} (Min.) $\leq V_{IN} \leq V_{DD}$	—	85	mA
	MB81P643287-60				75	
Power Down Current		I_{DD2P}	CKE = V_{IL} , $t_{CK} = \text{Min.}$ All banks idle, $0V \leq V_{IN} \leq V_{DD}$	—	35	mA
Active Standby Current (Power Supply Current)	MB81P643287-50	I_{DD3N}	CKE = V_{IH} , $t_{CK} = \text{Min.}$ All banks Active, NOP commands only, Input signals (except to CMD) are changed one time during 20 ns $0V \leq V_{IN} \leq V_{IL}$ (Max.), V_{IH} (Min.) $\leq V_{IN} \leq V_{DD}$	—	260	mA
	MB81P643287-60				225	

(Continued)

(Continued)

Parameter		Symbol	Condition	Value		Unit
				Min.	Max.	
Burst Read Current (Average Power Supply Current)	MB81P643287-50	I_{DD4R}	Burst Length = 4, CAS Latency = 3, All bank active, Gapless data, $t_{CK} = \text{Min.}$, $0 \text{ V} \leq V_{IN} \leq V_{IL} (\text{Max.})$, $V_{IH} (\text{Min.}) \leq V_{IN} \leq V_{DD}$	—	535	mA
	MB81P643287-60				460	
Burst Write Current (Average Power Supply Current)	MB81P643287-50	I_{DD4W}	Burst Length = 4, CAS Latency = 3, All bank active, Gapless data, $t_{CK} = \text{Min.}$, $0 \text{ V} \leq V_{IN} \leq V_{IL} (\text{Max.})$, $V_{IH} (\text{Min.}) \leq V_{IN} \leq V_{DD}$	—	595	mA
	MB81P643287-60				505	
Auto-refresh Current (Average Power Supply Current)	MB81P643287-50	I_{DD5}	Auto-refresh; $t_{CK} = \text{Min.}$, $0 \text{ V} \leq V_{IN} \leq V_{IL} (\text{Max.})$, $V_{IH} (\text{Min.}) \leq V_{IN} \leq V_{DD}$	—	320	mA
	MB81P643287-60				270	
Self-refresh Current (Average Power Supply Current)		I_{DD6}	Self-refresh; $\text{CKE} = V_{IL}$, $0 \text{ V} \leq V_{IN} \leq V_{DD}$	—	5	mA

- Notes: *1. All voltages referenced to V_{SS} .
*2. DC characteristics are measured after following the POWER-UP INITIALIZATION procedure.
*3. I_{DD} depends on the output termination or load conditions, clock cycle rate, and number of address and command change within certain period. The specified values are obtained with the output open.

MB81P643287-50/-60

■ AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note *1,*2,*3

AC PARAMETERS (CAS LATENCY DEPENDENT)

Parameter	Symbol		MB81P643287-50		MB81P643287-60		Unit
			Min.	Max.	Min.	Max.	
Clock Period	t_{CK}	CL = 3	5.0	9.0	6.0	10.5	ns
		CL = 2	7.5	10.5	9.0	10.5	

Parameter	Notes	Symbol	MB81P643287-50		MB81P643287-60		Unit
			Min.	Max.	Min.	Max.	
Input Setup Time (Except for DQS, DM and DQs)	*4	t_{IS}	1.0	—	1.2	—	ns
Input Hold Time (Except for DQS, DM and DQs)	*4	t_{IH}	1.0	—	1.2	—	ns
DM and Data Input Setup Time	*5	t_{DS}	0.6	—	0.7	—	ns
DM and Data Input Hold Time	*5	t_{DH}	0.6	—	0.7	—	ns
DQS First Input Setup Time (Input Preamble Setup Time)	*6	t_{DSPRES}	0	—	0	—	ns
Last Data Output to CKE High Level Hold Time		t_{QCKEH}	0	—	0	—	ns
Input Transition Time	*7	t_T	0.1	0.8	0.1	0.9	ns
Precharge Power Down Exit and Self-refresh Exit Time	*4	t_{PDEX}	3.0	—	3.6	—	ns
Time between Refresh	*8	t_{REF}	—	32	—	32	ms
Time between Auto-refresh Command	*8	t_{AREF}	—	8.0	—	8.0	μs
Pause Time after Power-on		t_{PAUSE}	200	—	200	—	μs

AC PARAMETERS (FREQUENCY DEPENDANT) Note *9

Parameter	Notes	Symbol	Min.	Max.	Unit
Clock High Time	*4	t_{CH}	$0.45 \times t_{CK}$	—	ns
Clock Low Time	*4	t_{CL}	$0.45 \times t_{CK}$	—	ns
DQS Low to High Input Transition Setup Time from CLK	*4, *10	t_{DQSS}	$0.75 \times t_{CK}$	$1.25 \times t_{CK}$	ns
DQS Low Input Pulse Width		t_{DSL}	$0.4 \times t_{CK}$	—	ns
DQS High Input Pulse Width		t_{DSH}	$0.4 \times t_{CK}$	—	ns
DQS First Low Input Hold Time (Input Preamble Hold Time)	*4	t_{DSPREH}	$0.25 \times t_{CK}$	—	ns
DQS First Low Input Pulse Width (Input Preamble Pulse Width)		t_{DSPRE}	$0.4 \times t_{CK}$	—	ns
DQS Last Low Input Hold Time (Input Postamble Hold Time)		t_{DSPST}	$0.4 \times t_{CK}$	—	ns
DQS Access Time from Clock	*4	t_{QSCK}	$-0.1 \times t_{CK} - 0.2$	$0.1 \times t_{CK} + 0.2$	ns
DQS Output Valid Time		t_{QSV}	$0.3 \times t_{CK}$	—	ns
DQS Output in Low-Z (Output Preamble Setup Time)	*4, *11	t_{QSLZ}	$-0.1 \times t_{CK} - 0.2$	—	ns
DQS First Low Output Hold Time (Output Preamble Hold Time)	*4	t_{QSPRE}	$0.9 \times t_{CK} - 0.2$	$1.1 \times t_{CK} + 0.2$	ns
DQS Last Low Output Hold Time (Output Postamble Hold Time)	*4, *12	t_{QSPST}	$0.4 \times t_{CK} - 0.2$	$0.6 \times t_{CK} + 0.2$	ns
DQS Last Low Output in High-Z from CLK or $\overline{CLK}$	*12	t_{QSHZ}	—	$0.1 \times t_{CK} + 0.2$	ns
DQ Access Time from CLK & $\overline{CLK}$	*4	t_{ACC}	$-0.1 \times t_{CK} - 0.2$	$0.1 \times t_{CK} + 0.2$	ns
DQ Access Time from DQS	*5	t_{QSQ}	$-0.1 \times t_{CK}$	$0.1 \times t_{CK}$	ns
DQ Output Data Valid Time from DQS		t_{DV}	$0.3 \times t_{CK}$	—	ns
DQ Output in Low-Z	*4, *11	t_{LZ}	$-0.1 \times t_{CK} - 0.2$	—	ns
DQ Output in High-Z	*4, *12	t_{HZ}	$-0.1 \times t_{CK} - 0.2$	$0.1 \times t_{CK} + 0.2$	ns
DQ & DM Input Pulse Width		t_{DIPW}	$0.4 \times t_{CK}$	—	ns
DQS Falling Edge to Clock Hold Time		t_{DSCH}	$0.2 \times t_{CK}$ (1.5 ns Min.)	—	ns
DQS Falling Edge to Clock Setup Time		t_{DSCS}	$0.2 \times t_{CK}$ (1.5 ns Min.)	—	ns

MB81P643287-50/-60

EXAMPLE OF FREQUENCY DEPENDANT AC PARAMETERS (@ Minimum t_{CK})

Parameter	Symbol	$t_{CK} = 5ns$		$t_{CK} = 6ns$		$t_{CK} = 7.5ns$		$t_{CK} = 9ns$		$t_{CK} = 10.5ns$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock High Time	t_{CH}	2.3	—	2.7	—	3.4	—	4.1	—	4.8	—	ns
Clock Low Time	t_{CL}	2.3	—	2.7	—	3.4	—	4.1	—	4.8	—	ns
DQS Low to High Input Transition Setup Time from CLK	t_{DQSS}	3.8	6.3	4.5	7.5	5.7	9.4	6.8	11.3	7.9	13.2	ns
DQS Low Input Pulse Width	t_{DSL}	2.0	—	2.4	—	3.0	—	3.6	—	4.2	—	ns
DQS High Input Pulse Width	t_{DSH}	2.0	—	2.4	—	3.0	—	3.6	—	4.2	—	ns
DQS First Low Input Hold Time (Input Preamble Hold Time)	t_{DSPREH}	1.3	—	1.5	—	1.9	—	2.3	—	2.7	—	ns
DQS First Low Input Pulse Width (Input Preamble Pulse Width)	t_{DSPRE}	2.0	—	2.4	—	3.0	—	3.6	—	4.2	—	ns
DQS Last Low Input Hold Time (Postamble Hold Time)	t_{DSPST}	2.0	—	2.4	—	3.0	—	3.6	—	4.2	—	ns
DQS Access Time from Clock	t_{QSCk}	-0.7	0.7	-0.8	0.8	-1.0	1.0	-1.1	1.1	-1.3	1.3	ns
DQS Output Valid Time	t_{QSV}	1.5	—	1.8	—	2.3	—	2.7	—	3.2	—	ns
DQS Output in Low-Z (Output Preamble)	t_{QSLZ}	-0.7	—	-0.8	—	-1.0	—	-1.1	—	-1.3	—	ns
DQS First Low Output Hold Time (Output Preamble)	t_{QSPRE}	4.3	5.7	5.2	6.8	6.6	8.5	7.9	10.1	9.3	11.8	ns
DQS Last Low Output Hold Time (Output Postamble)	t_{QSPST}	1.8	3.2	2.2	3.8	2.8	4.7	3.4	5.6	4.0	6.5	ns
DQS Last Low Output in High-Z from CLK or $\overline{CLK}$	t_{QSHZ}	—	0.7	—	0.8	—	1.0	—	1.1	—	1.3	ns
DQ Output Access Time from CLK & $\overline{CLK}$	t_{ACC}	-0.7	0.7	-0.8	0.8	-1.0	1.0	-1.1	1.1	-1.3	1.3	ns
DQ Output Access Time from DQS	t_{QSQ}	-0.5	0.5	-0.6	0.6	-0.8	0.8	-0.9	0.9	-1.1	1.1	ns
DQ Output Data Valid Time from DQS	t_{DV}	1.5	—	1.8	—	2.3	—	2.7	—	3.2	—	ns
DQ Output in Low-Z	t_{LZ}	-0.7	—	-0.8	—	-1.0	—	-1.1	—	-1.3	—	ns
DQ Output in High-Z	t_{HZ}	-0.7	0.7	-0.8	0.8	-1.0	1.0	-1.1	1.1	-1.3	1.3	ns
DQ & DM Input Pulse Width	t_{DIPW}	2.0	—	2.4	—	3.0	—	3.6	—	4.2	—	ns
DQS Falling Edge to Clock Hold Time	t_{DSCH}	1.5	—	1.5	—	1.5	—	1.8	—	2.1	—	ns
DQS Falling Edge to Clock Setup Time	t_{DSCS}	1.5	—	1.5	—	1.5	—	1.8	—	2.1	—	ns

LATENCY

(The latency values on these parameters are fixed regardless of clock period.)

Parameter	Notes	Symbol	MB81P643287-50		MB81P643287-60		Unit
			Min.	Max.	Min.	Max.	
$\overline{\text{RAS}}$ Cycle Time *13	CL = 3	I_{RC}	6	—	6	—	t_{CK}
	CL = 2		5	—	5	—	t_{CK}
$\overline{\text{RAS}}$ Active Time	CL = 3	I_{RAS}	4	11000	4	11000	t_{CK}
	CL = 2		3	7333	3	7333	t_{CK}
$\overline{\text{RAS}}$ Precharge Time		I_{RP}	2	—	2	—	t_{CK}
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	CL = 3	I_{RCD}	3	—	3	—	t_{CK}
	CL = 2		2	—	2	—	t_{CK}
$\overline{\text{RAS}}$ to $\overline{\text{RAS}}$ Bank Active Delay Time		I_{RRD}	1	—	1	—	t_{CK}
Precharge All Bank to Active	CL = 3	I_{RPA}	4	—	4	—	t_{CK}
	CL = 2		3	—	3	—	t_{CK}
Read Command to Write Command Delay	CL = 3	I_{RWD}	BL/2+3	—	BL/2+3	—	t_{CK}
	CL = 2		BL/2+2	—	BL/2+2	—	t_{CK}
Last Input Data to Read Command Delay *14		I_{WRD}	2.5	—	2.5	—	t_{CK}
Last Input Data to Precharge Command Lead Time *14		I_{DPL}	2.5	—	2.5	—	t_{CK}
Write with Auto Precharge Command to Active command Delay *14		I_{WAL}	BL/2+3+ I_{RP}	—	BL/2+3+ I_{RP}	—	t_{CK}
Mode Register Access to Next Command Input Delay		I_{MRD}	2	—	2	—	t_{CK}
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ Delay		I_{CCD}	1	—	1	—	t_{CK}
$\overline{\text{CAS}}$ Bank Delay		I_{CBD}	1	—	1	—	t_{CK}
Precharge Power Down Exit to Next Command Input Delay		I_{PDEXP}	2	—	2	—	t_{CK}
Minimum Stable Clock Input After Self-refresh Exit Before READ Command Input *15		I_{SCD}	400	—	400	—	t_{CK}
Minimum Stable Clock Input After Self-refresh Exit Before non-READ Command Input		I_{XSNR}	12	—	12	—	t_{CK}
Minimum Stable Clock Input for DLL Lock-on in Power-up Initialization sequence. *16	$t_{\text{CK}} \leq 7.5\text{ns}$	I_{PCD}	400	—	400	—	t_{CK}
	$t_{\text{CK}} \leq 10.5\text{ns}$		630	—	630	—	t_{CK}
Auto-refresh Cycle Time		I_{RFC}	12	—	12	—	t_{CK}

MB81P643287-50/-60

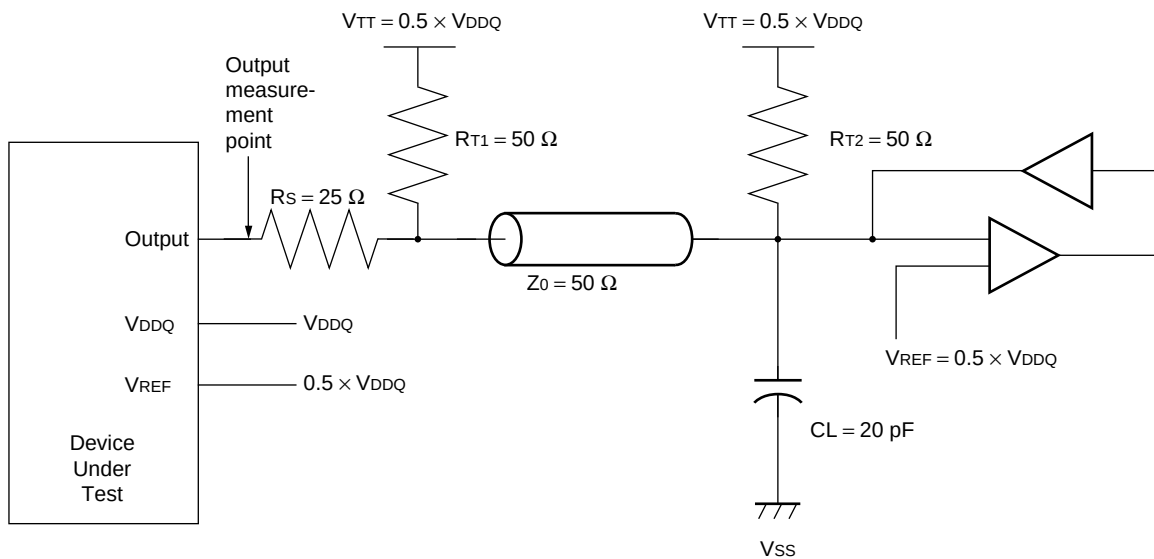
LATENCY - FIXED VALUES

(The latency values on these parameters are fixed regardless of clock period.)

Parameter	Notes	Symbol	MB81P643287-50	MB81P643287-60	Unit
BST Command to Output in High-Z	CL = 3	t _{BSH}	3	3	t _{CK}
	CL = 2		2	2	t _{CK}
BST Command to New Command Input *17	CL = 3	t _{BSNC}	3	3	t _{CK}
	CL = 2		2	2	t _{CK}
DM to Input Data Delay		t _{DQD}	0	0	t _{CK}
Precharge to Output in High-Z	CL = 3	t _{ROH}	3	3	t _{CK}
	CL = 2		2	2	t _{CK}
CKE Low to Command/Address Input Inactive		t _{CKE}	1	1	t _{CK}

- Notes:
- *1. AC characteristics are measured after following the POWER-UP INITIALIZATION procedure and stable clock input with constant clock period and with 50% duty cycle.
 - *2. Access Times assume input slew rate of 1ns/volt between $V_{REF}+0.35V$ to $V_{REF}-0.35V$, where V_{REF} is $V_{DDQ}/2$, with SSTL_2 output load conditions. Refer to AC TEST LOAD CIRCUIT.
 - *3. $V_{REF} = 1.25V$ is a typical reference level for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{Min.})$ and $V_{IL}(\text{Max.})$ unless otherwise noted. Refer to AC TEST CONDITIONS.
 - *4. This parameter is measured from the cross point of CLK and $\overline{\text{CLK}}$ input.
 - *5. This parameter is measured from signal transition point of DQS_0 to DQS_3 input crossing V_{REF} level.
 - *6. The specific requirement is that DQS be valid (HIGH or LOW) on or before this CLK edge. The case shown (DQS going from High-Z to logic LOW) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be HIGH at this time, depending on t_{DSS} .
 - *7. t_T is defined as the transition time between $V_{IH(AC)}(\text{Min.})$ and $V_{IL(AC)}(\text{Max.})$.
 - *8. Total of 4096 REF command must be issued within $t_{REF}(\text{Max.})$. t_{AREF} is a reference value for distributed refresh and specifies the time between one REF command to next REF command except for a condition where $CKE = \text{Low}$ during Self-refresh mode.
 - *9. This parameter is scalable by actual clock period (t_{CK}) and affected by an abrupt change of duty cycle, jitters on clock input, T_A and level of V_{DD} and V_{DDQ} . The internal DLL circuit can adjust delay time against the change of following condition :
 - $T_A \leq 0.1^\circ\text{C} / 20 \text{ ns},$
 - $V_{DD} \leq 1 \text{ mV} / 10 \text{ ns},$
 - $V_{DDQ} \leq 1 \text{ mV} / 10 \text{ ns},$
 if change rate is bigger than these values, frequency dependent AC parameters affected by DLL jitters.
 - *10. More than 2 signal edge of DQS_0 to DQS_3 should not be input within 1 clock (t_{CK}) cycle.
 - *11. Low-Z (Low Impedance State) is specified and measured at $V_{TT} \pm 200\text{mV}$.
 - *12. t_{QSPST} , t_{QSHZ} and t_{HZ} are specified where output buffer is no longer driven.
 - *13. Actual clock count of I_{RC} will be sum of clock count of I_{RAS} and I_{RP} .
 - *14. Assume $t_{DQSS} = 1 \times t_{CK}$. If actual t_{DQSS} is within specified minimum and maximum range, those parameters can be assumed $t_{DQSS} = 1 \times t_{CK}$.
 - *15. Applicable also if device operating conditions such as supply voltages, case temperature, and/or clock frequency (t_{CK} difference must be 0.2 ns or less) is changed during any operation.
 - *16. Clock period must satisfy specified t_{CK} and it must be stable.
 - *17. Assume BST is effective to read operation (issued prior to the end of burst read).

Fig. 5 - AC TEST LOAD CIRCUIT (SSTL_2, Class II)



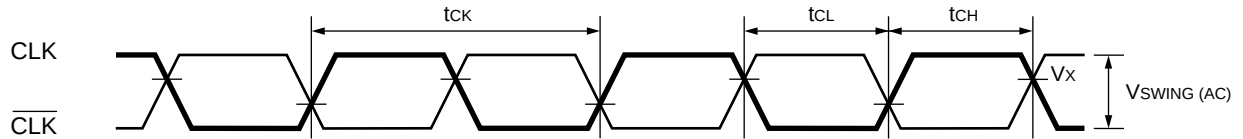
Note: AC characteristics are measured in this condition. This load circuit is not applicable for DC Test.

AC TEST CONDITIONS

Parameters	Symbol	Value	Unit
Single-end Input			
Input High Level	V_{IH}	$V_{REF} + 0.35$	V
Input Low Level	V_{IL}	$V_{REF} - 0.35$	V
Input Reference Level	V_{REF}	$V_{DDQ} / 2$	V
Input Slew Rate	SLEW	1.0	V/ns
Differential Input (CLK and $\overline{CLK}$)			
Input Reference Level	V_r	$V_{X(AC)}^*$	V
Input Level	V_{SWING}	0.7	V
Input Slew Rate	SLEW	1.0	V/ns

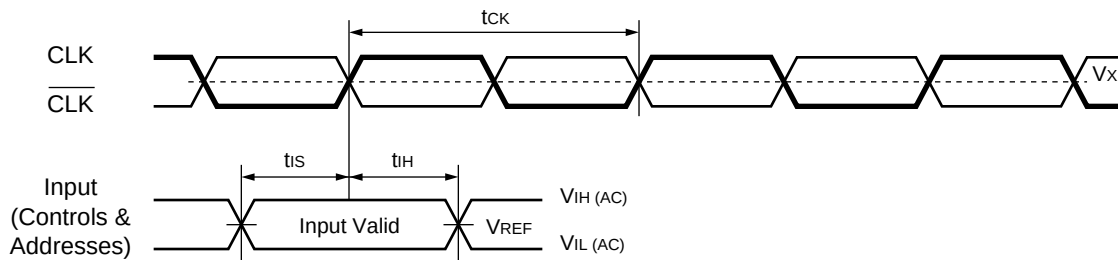
* : V_x means the actual cross point between CLK and $\overline{CLK}$ input.

Fig. 6 - AC TIMING of CLK & $\overline{\text{CLK}}$



Note: Reference level for AC timings of clock are the cross point of CLK and $\overline{\text{CLK}}$ as specified in V_x .

Fig. 7 - AC TIMING of Command Input & Address



Note: The cross point of CLK and $\overline{\text{CLK}}$ (V_x) is used for command and address input.
The reference level of single ended input is V_{REF} .

Fig. 8 - AC TIMING of Write Mode (Data Strobe, Write Data and Data Mask Input)

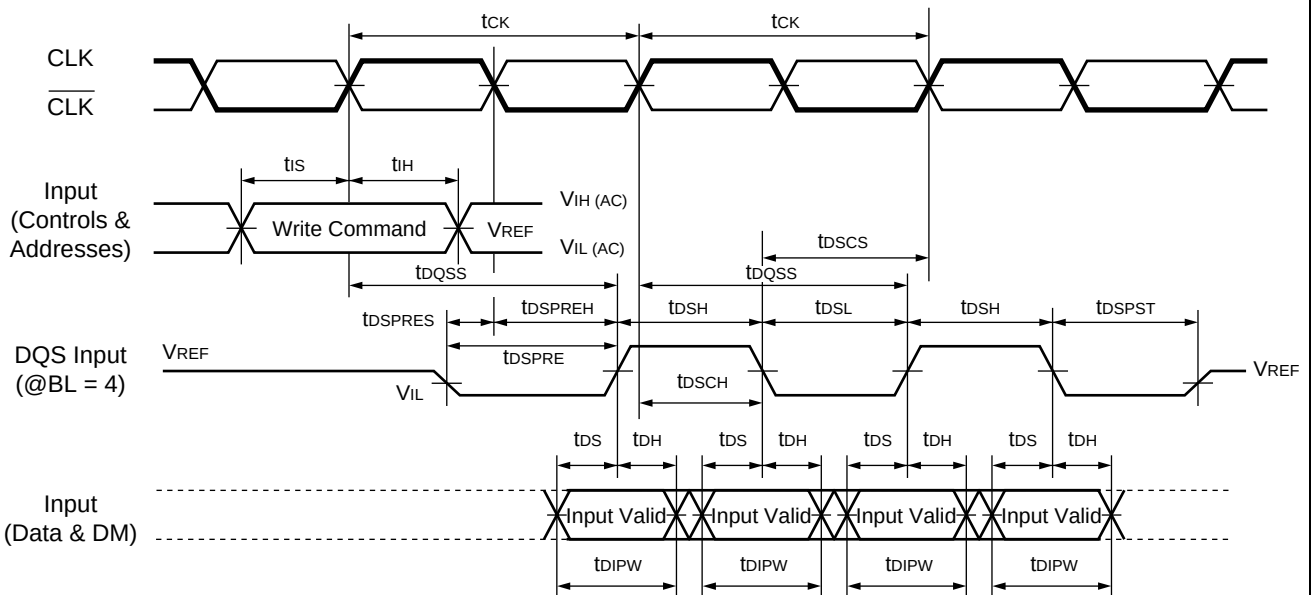
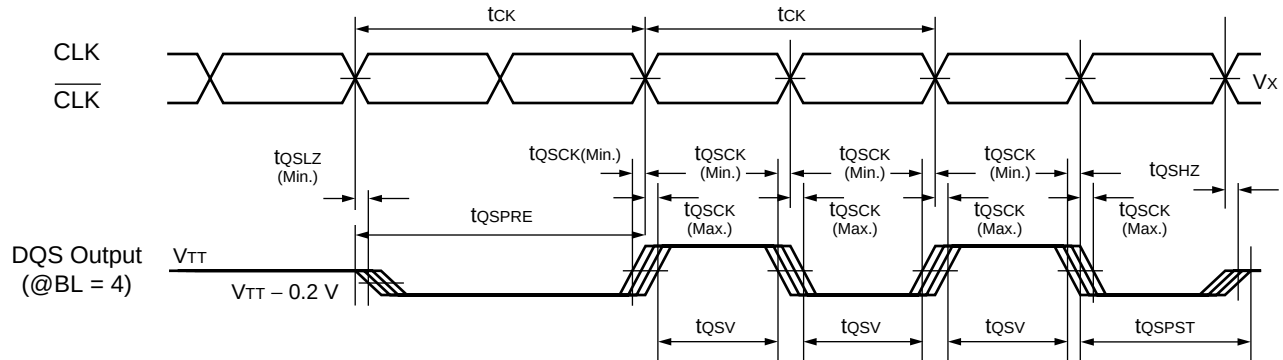
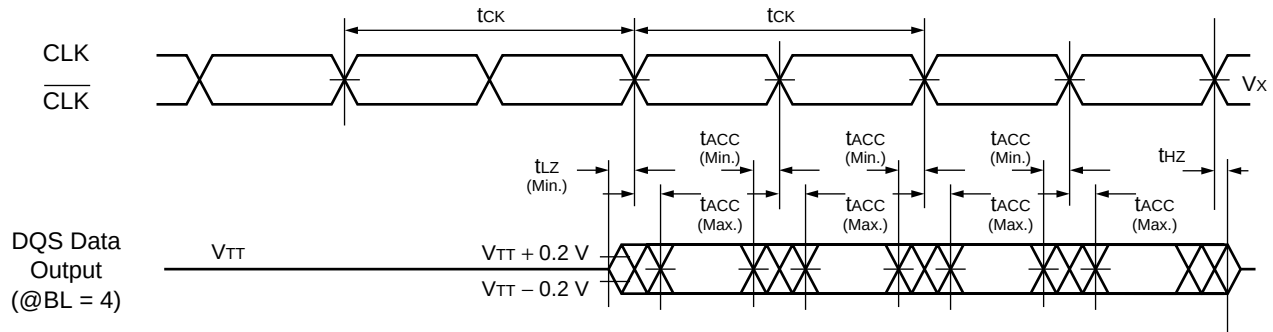


Fig. 9 - AC TIMING of Read Mode (Clock to DQS Output Delay Time)



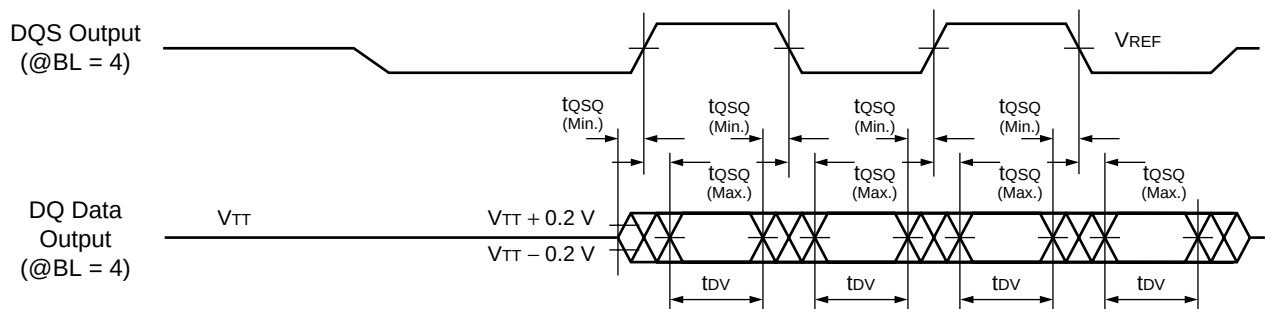
Note: DQS Access time (t_{QSK}) is measured from the cross point of clock (V_x) and V_{REF} .
The end of t_{QSPST} and t_{QSHZ} specification is defined at where output buffer is no longer driven.

Fig. 10 - AC TIMING of Read Mode (Clock to Data Output Delay Time)



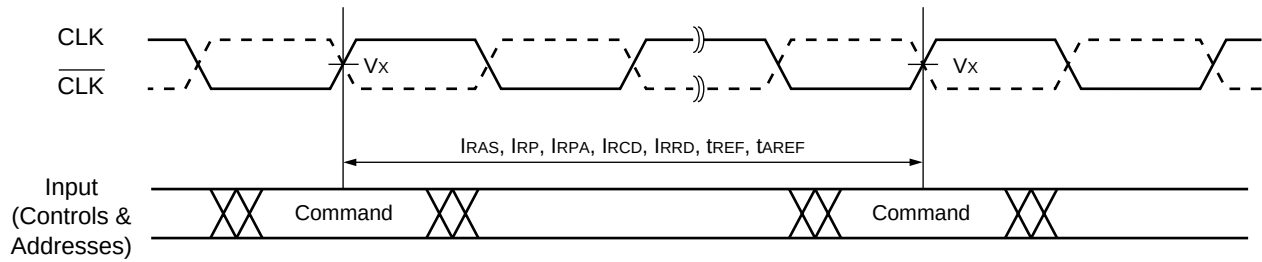
Note: Access time (t_{ACC}) is measured from the cross point of clock (V_x) and V_{REF} .
The end of t_{HZ} specification is defined at where output buffer is no longer driven.

Fig. 11 - AC TIMING of Read Mode (DQS Output to Data Output Delay Time)



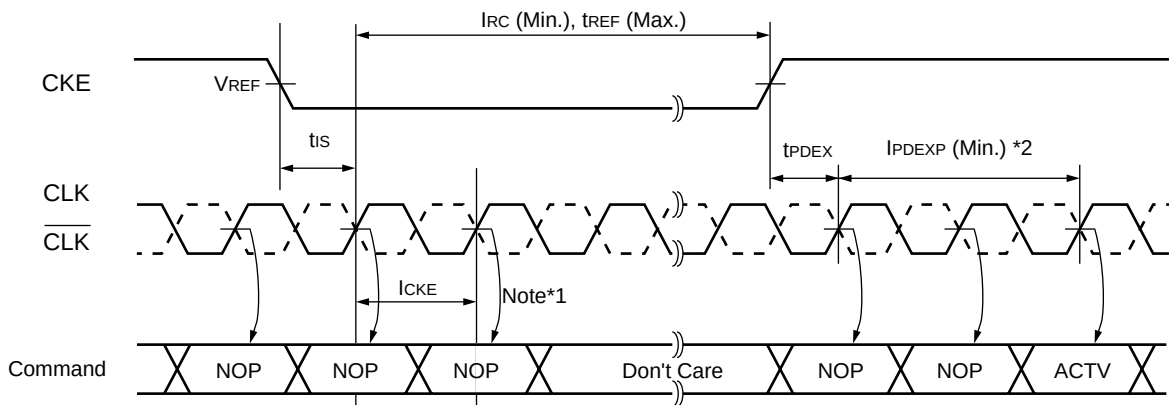
Note: DQS Output Edge to Data Output Edge Skew Time (t_{QSQ}) is measured from V_{TT} to V_{TT} .

Fig. 12 - AC TIMING, PULSE WIDTH



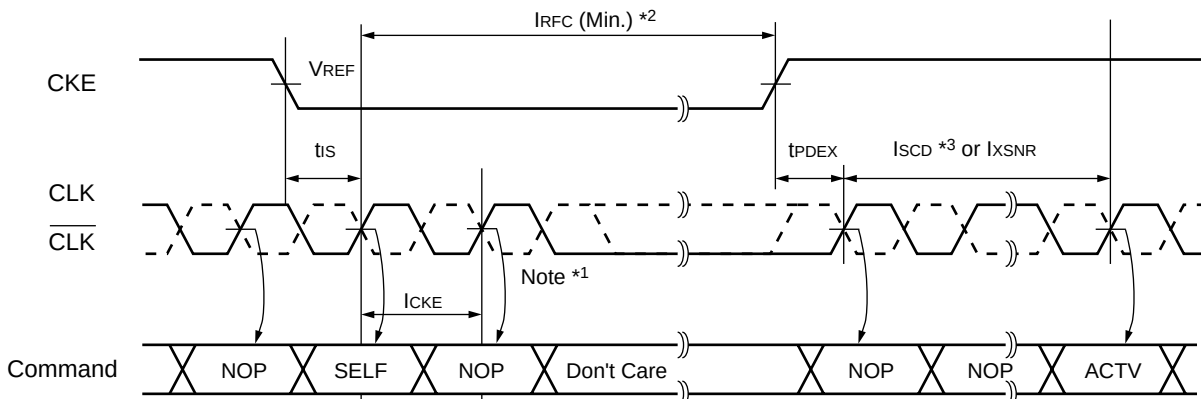
Note: All parameters listed above are measured from the cross point at rising edge of the CLK and falling edge of $\overline{\text{CLK}}$ of one command input to next command input.

Fig. 13 - AC TIMING of Precharge Power Down Mode



Notes: *1. Minimum 2 clock cycles is required for complete power down on clock buffer.
*2. If either any supply voltage or clock input condition is changed from the previous operating condition (other than PDEN and REF), I_{SCD} must be satisfied prior to any command input.

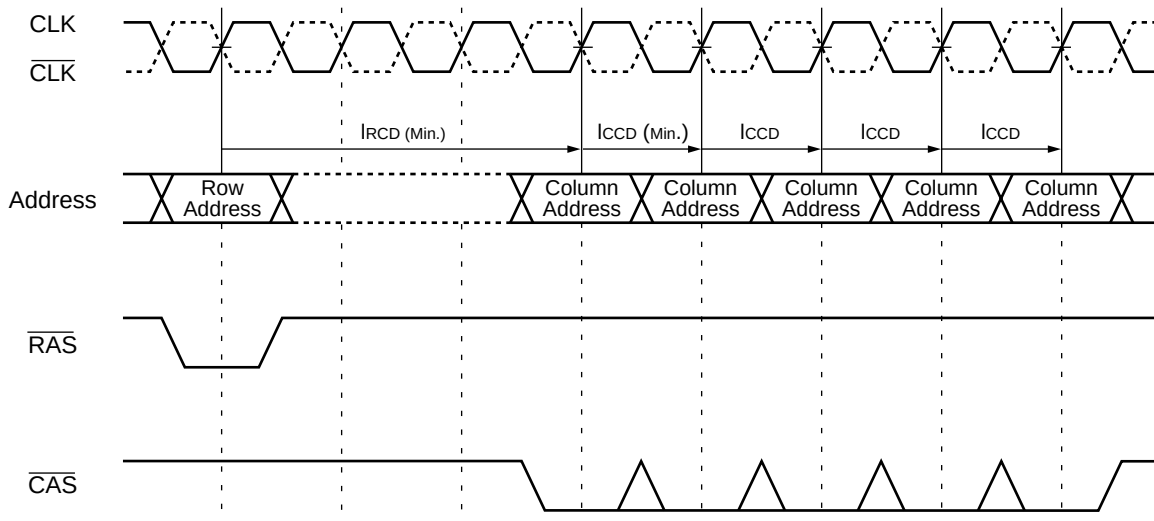
Fig. 14 - AC TIMING of Self-refresh Mode



Notes: *1. Minimum 2 clock cycles is required for complete power down on clock buffer.
*2. CKE must maintain High level and clock must be provided during the I_{SCD} period. I_{SCD} must be satisfied before read command input.
*3. I_{SCD} must be satisfied before read command input.

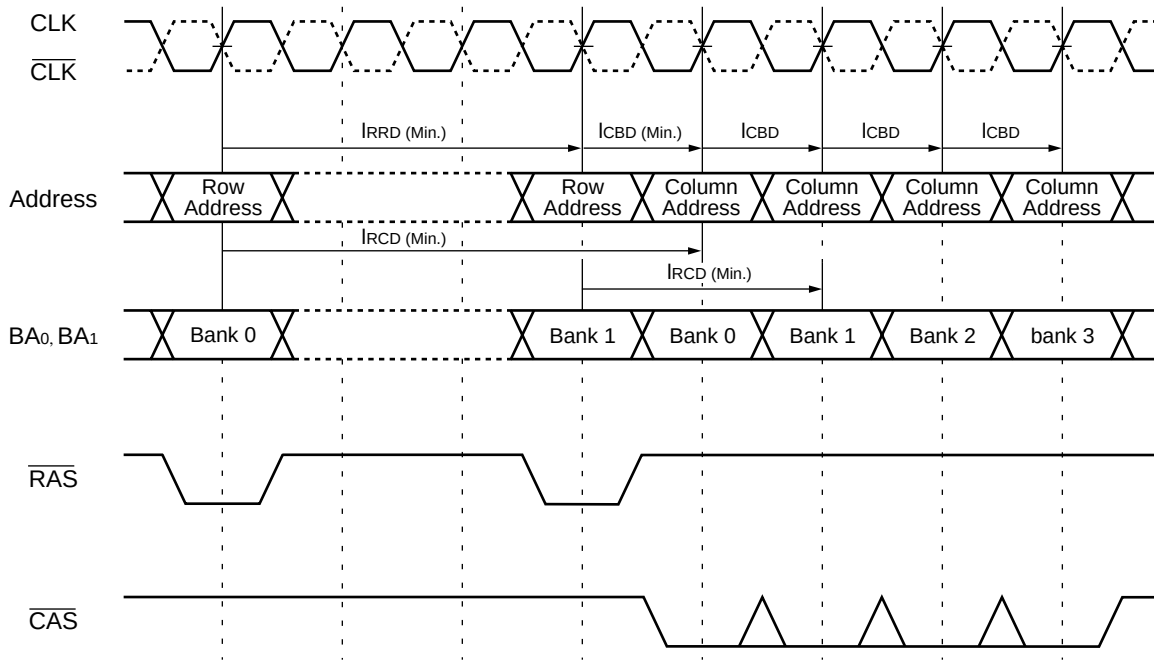
■ TIMING DIAGRAMS

TIMING DIAGRAM - 1: COLUMN ADDRESS TO COLUMN ADDRESS INPUT DELAY

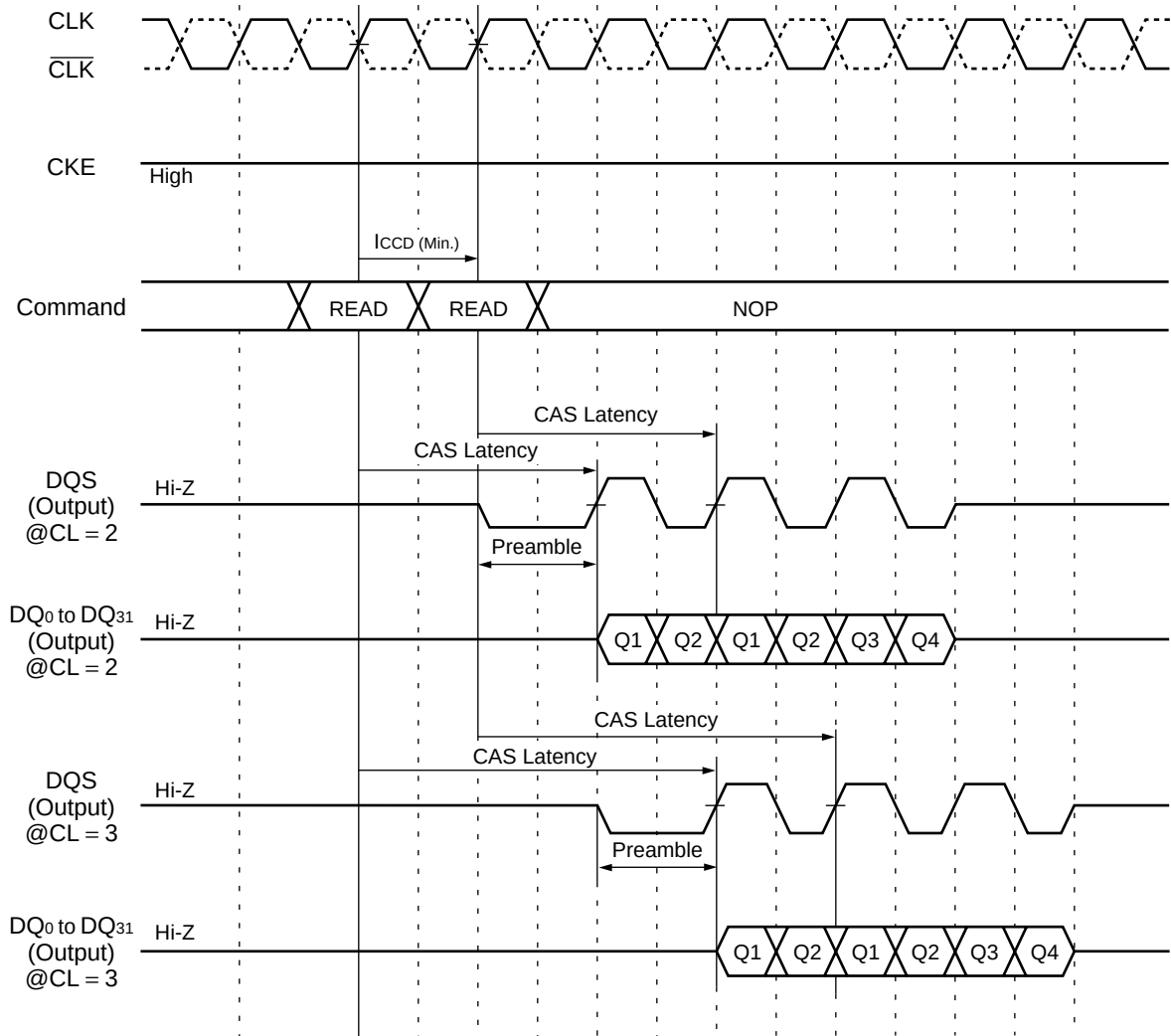


Note: t_{CCD} , $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ address delay, is applicable to the same bank access and it can be one or more clock period.

TIMING DIAGRAM - 2: DIFFERENT BANK ADDRESS INPUT DELAY

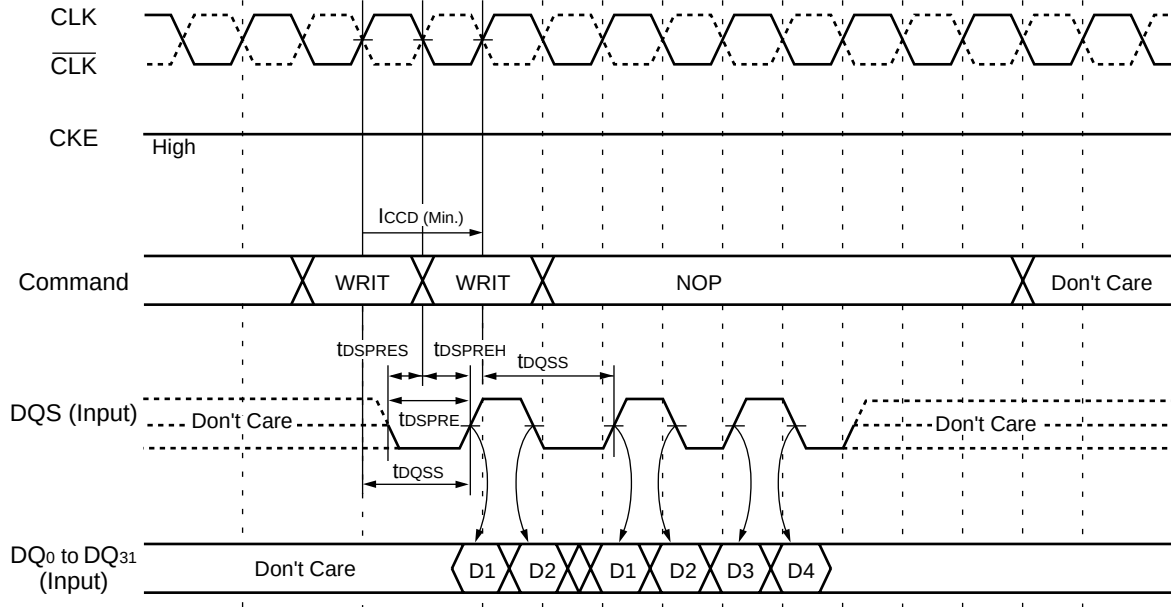


TIMING DIAGRAM - 3: READ (EXAMPLE @ BL = 4)



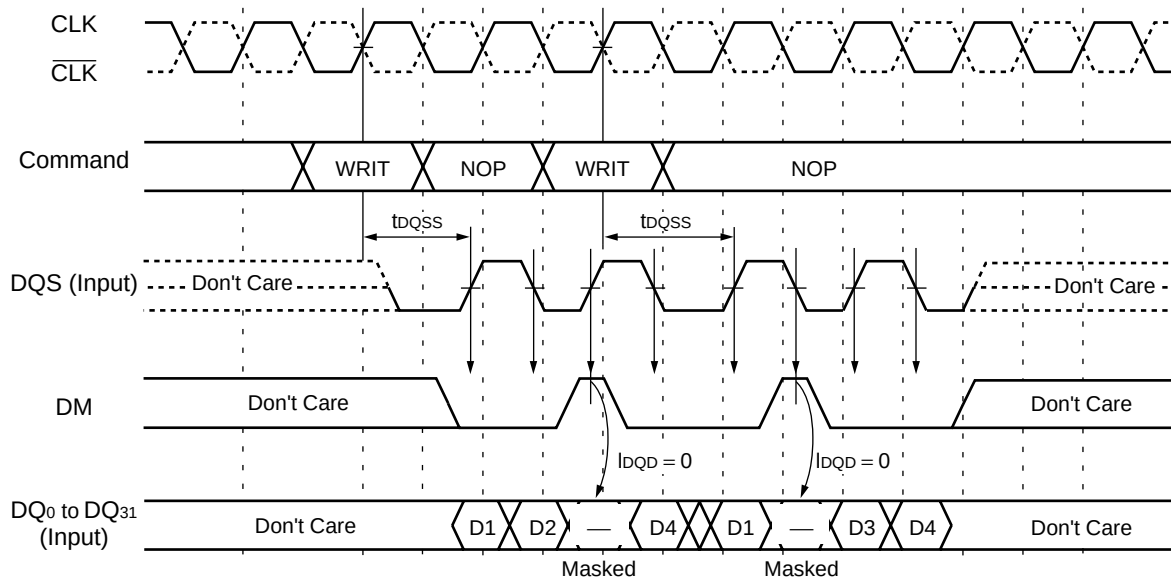
Note: CAS Latency is defined from Read command to first rising edge of DQS₀ to DQS₃ output.
Preamble is $1 \times t_{CK}$ length and starts driving Low level.

TIMING DIAGRAM - 4: WRITE (EXAMPLE @ BL = 4)



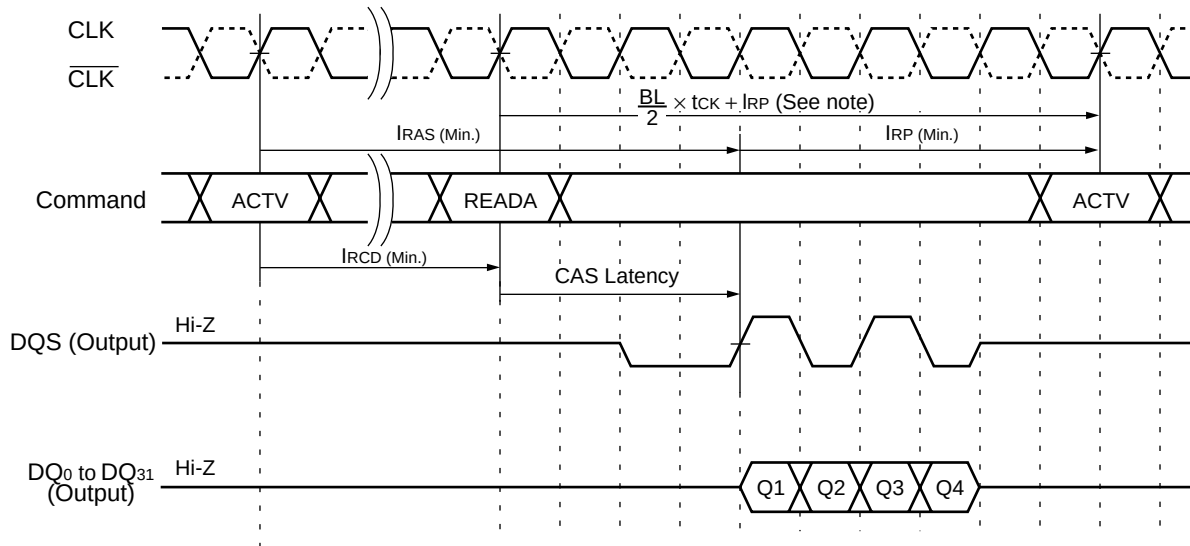
Note: DQS Setup Time, t_{DQSS} , must be within a range of $0.75 \cdot t_{\text{CK}}$ to $1.25 \cdot t_{\text{CK}}$ from write command Input.

TIMING DIAGRAM - 5: DM, WRITE DATA MASK (EXAMPLE @ BL = 4)



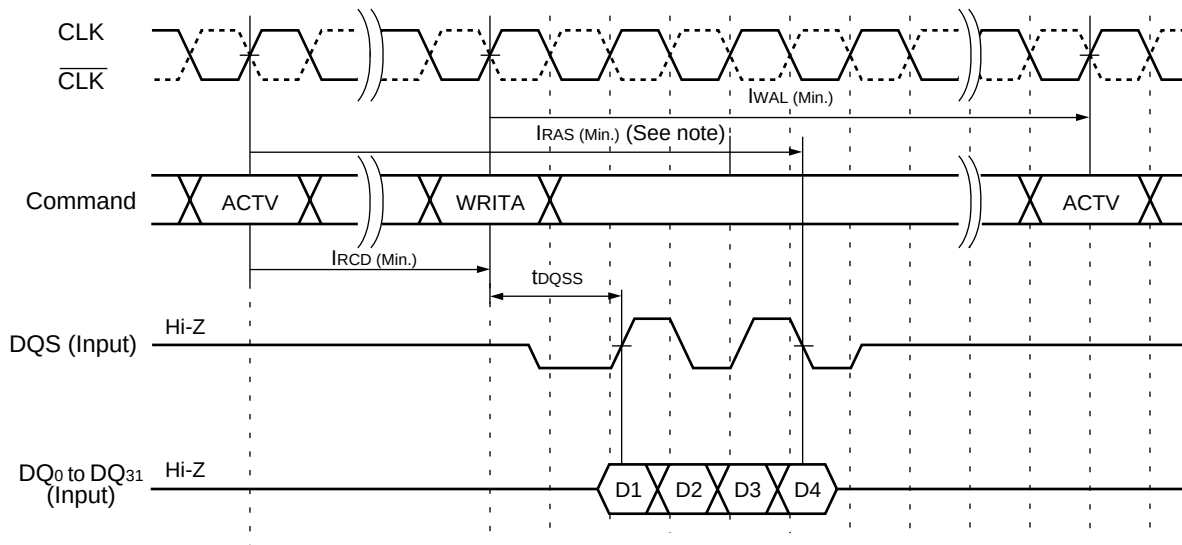
Note: DM are latched by DQS Input together with Data Input after write command.

**TIMING DIAGRAM - 6: READ WITH AUTO-PRECHARGE
(EXAMPLE @ CL = 2.0, BL = 4 Applied to same bank)**



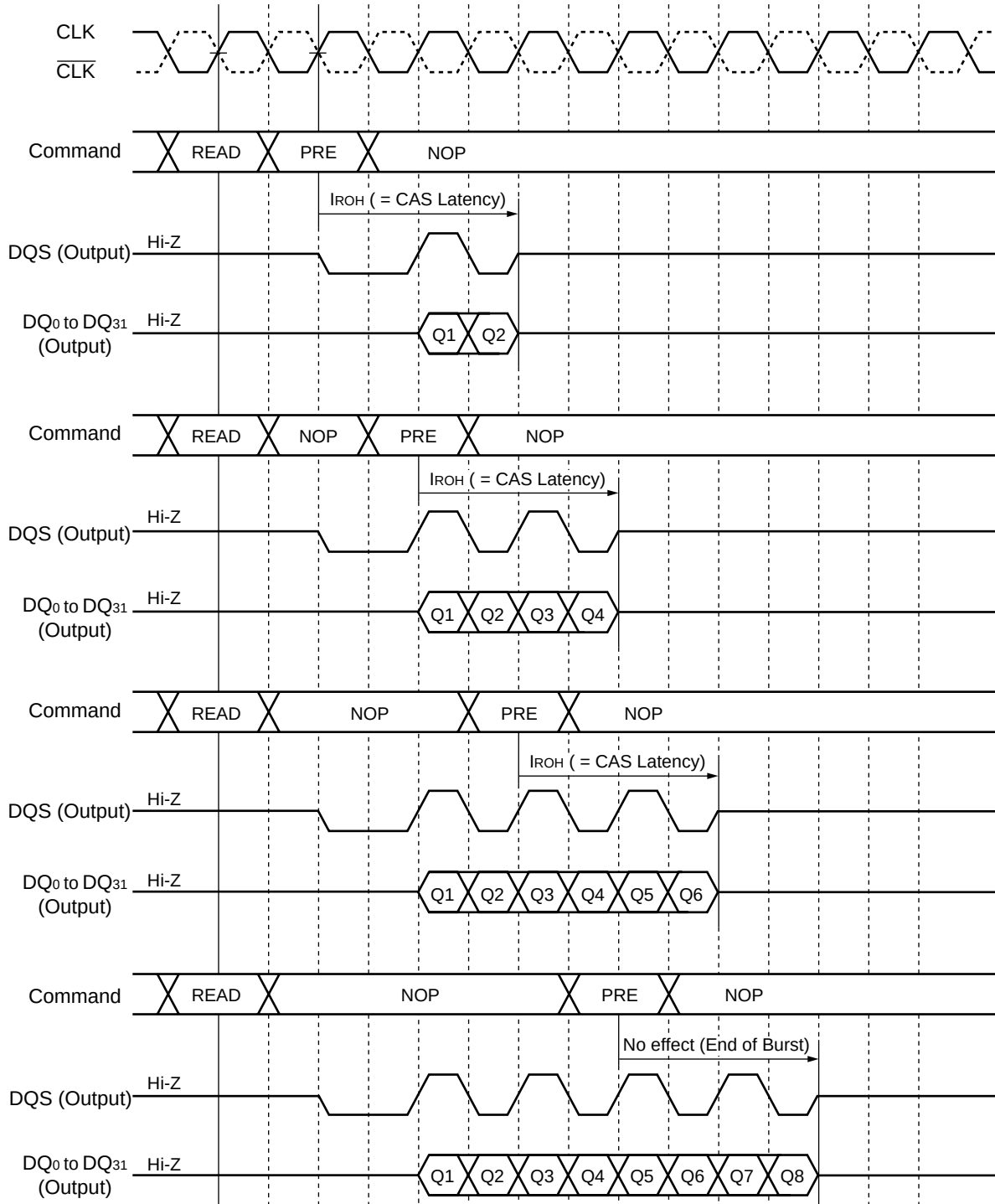
Note: Internal precharge operation at Read with Auto-precharge command (READA) is started BL/2 clock later from READA command.
 If BL=2, the READA command should not be issued no earlier than 1 clock (BL/2 = 1) before I_{RA}S (Min.).
 If BL=4, the READA command should not be issued no earlier than 2 clock (BL/2=2) before I_{RA}S (Min.).

**TIMING DIAGRAM - 7: WRITE WITH AUTO-PRECHARGE
(EXAMPLE @ CL = 2.0, BL = 4 Applied to same bank)**



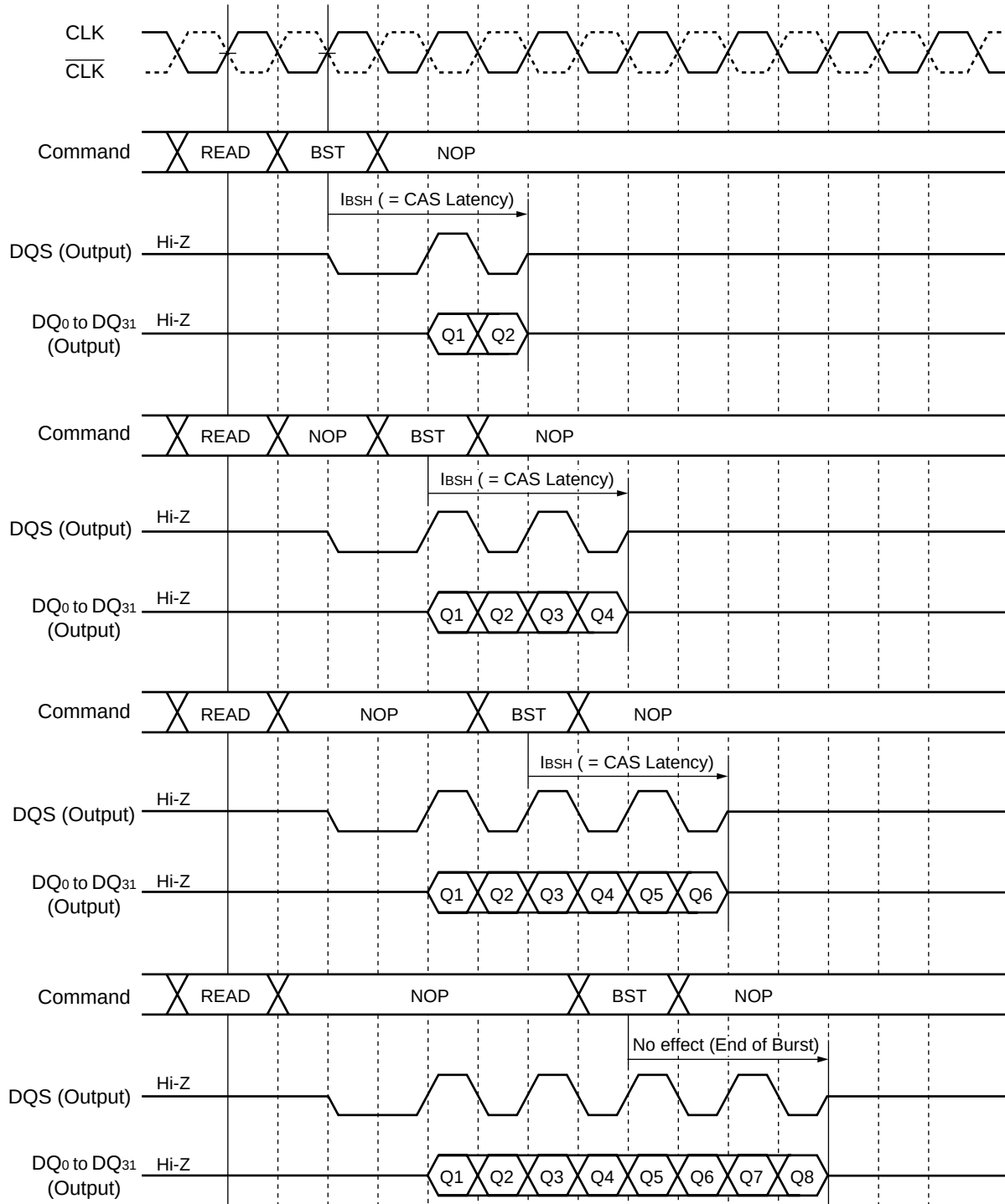
Note: Write with Auto-precharge command (WRITA) must be issued after I_{RC}D is satisfied and be considered to meet I_{RA}S requirement applied to end of burst length (BL) regardless of where it is masked or not.

**TIMING DIAGRAM - 8: READ INTERRUPTED BY PRECHARGE
(EXAMPLE @ CL = 2, BL = 8)**



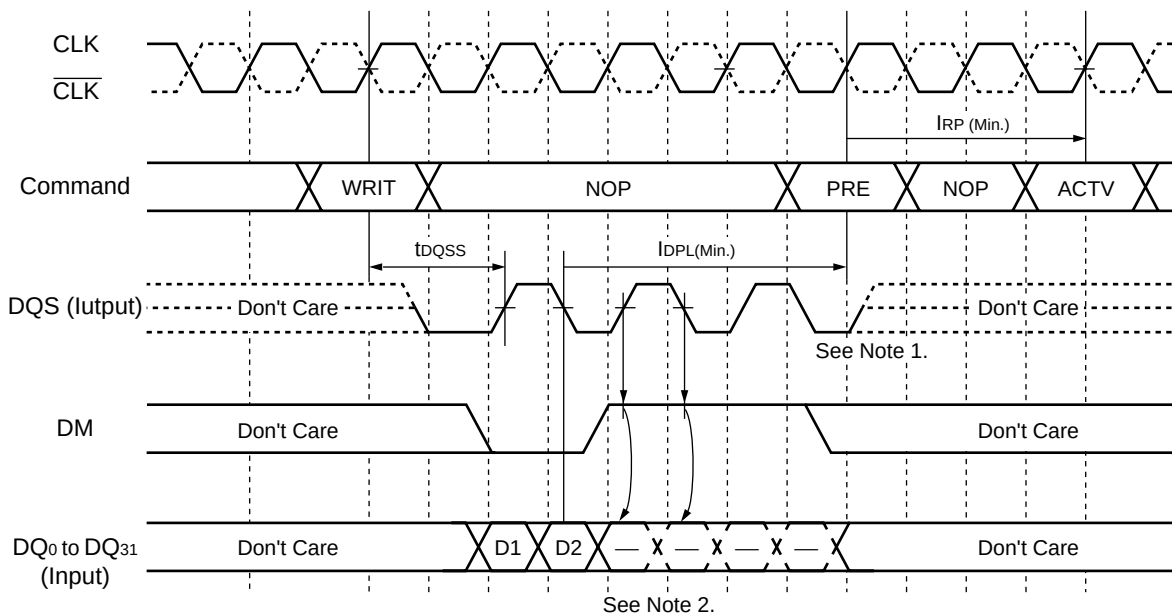
Note: I_{ROH} is the same as CAS Latency (CL). In case of CL = 3, the I_{ROH} is 3 clock.

**TIMING DIAGRAM - 9: READ INTERRUPTED BY BURST STOP
(EXAMPLE @ CL = 2, BL = 8)**



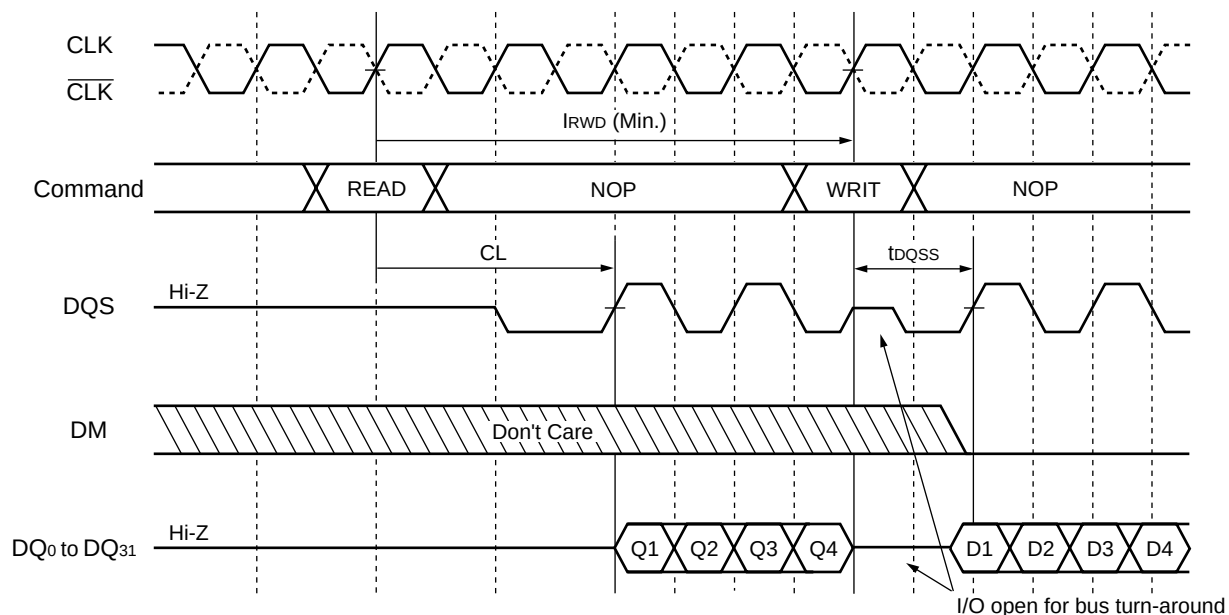
Note: I_{BSH} is the same as CAS Latency (CL). In case of CL = 3, the I_{BSH} is 3 clock.

TIMING DIAGRAM - 10: WRITE INTERRUPTED BY PRECHARGE (EXAMPLE @ CL = 2, BL = 8)



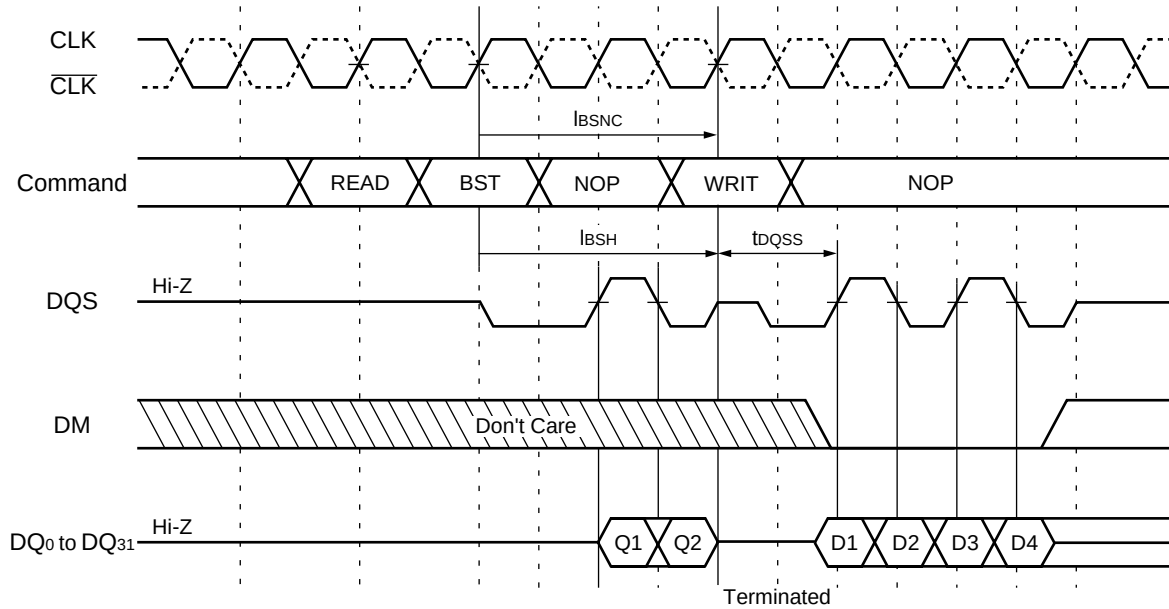
Note: 1. DQS Input are not required from when Precharge command is issued.
2. This pair of write data must be masked prior to Precharge command.

TIMING DIAGRAM - 11: READ TO WRITE (EXAMPLE @ CL = 2, BL = 4)



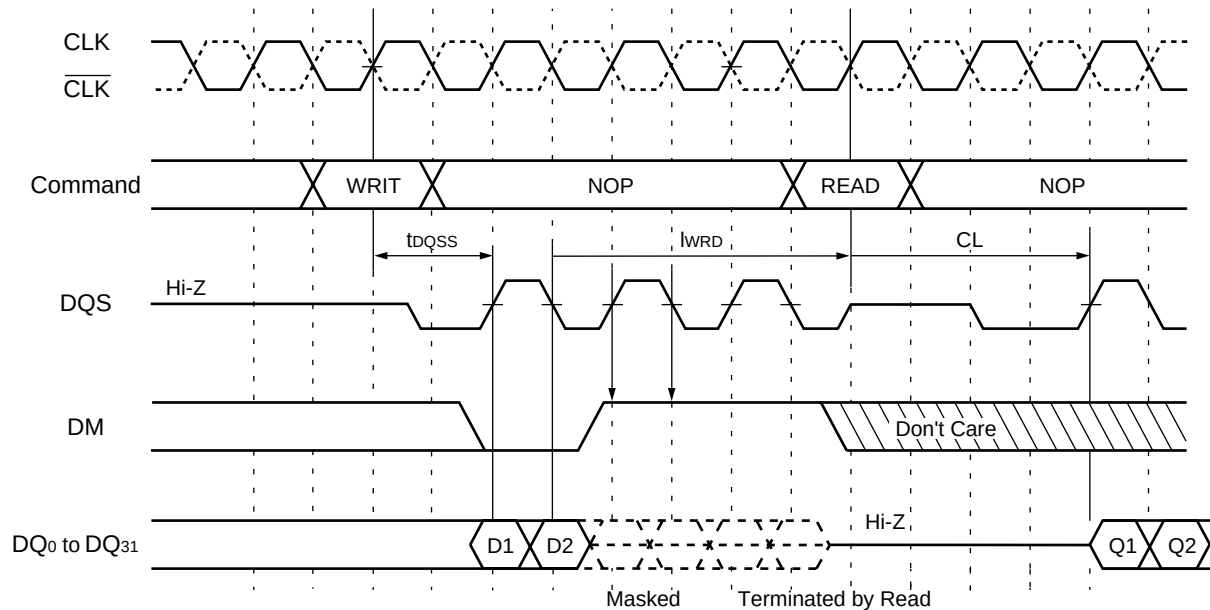
Note: IRWD defines a minimum delay from Read to Write command input applied to the same bank.

TIMING DIAGRAM - 12: READ TO WRITE (EXAMPLE @ CL = 2, BL = 4)



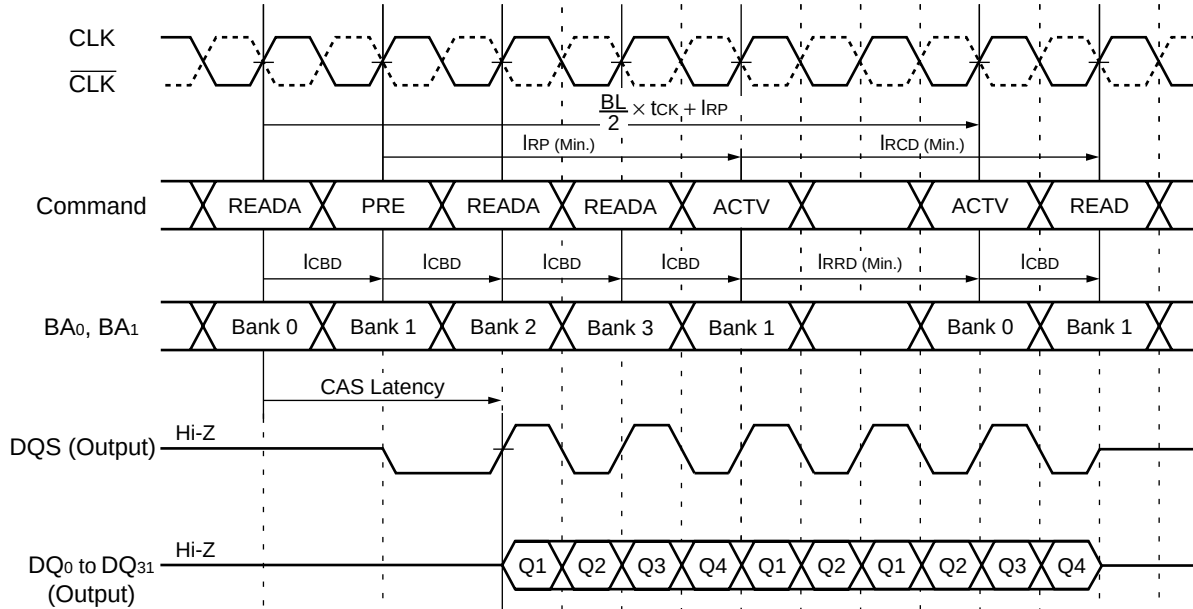
Note: DM are latched by DQS Input after Write command together with data Input.

TIMING DIAGRAM - 13: WRITE TO READ (EXAMPLE @ CL = 2, BL = 8)



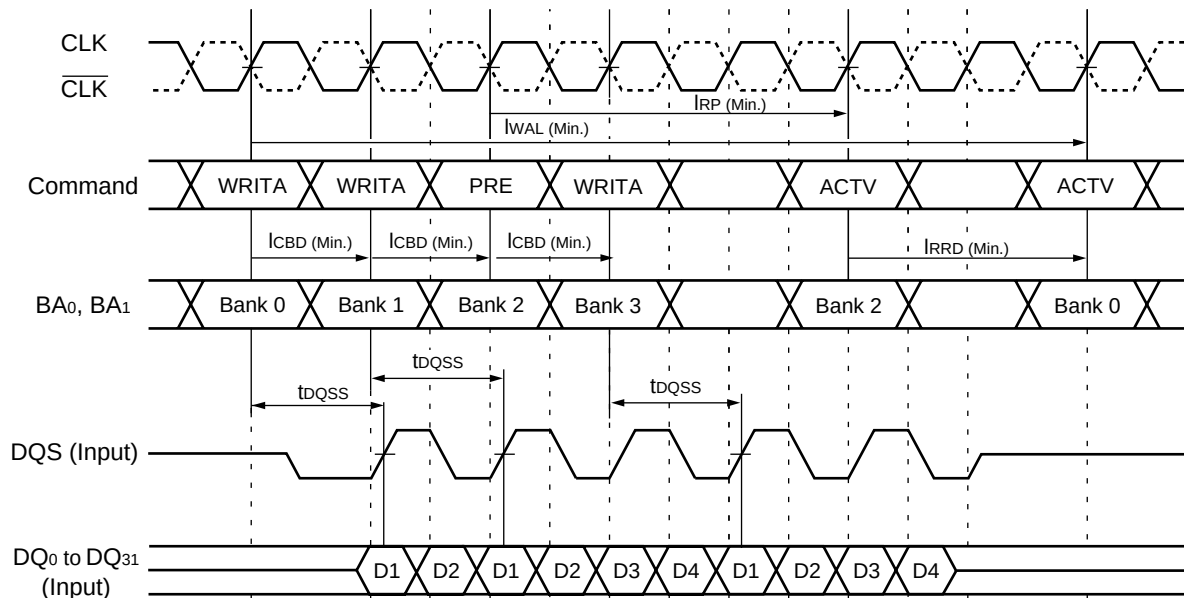
Note: Read command must be issued after l_{WRD} is satisfied and proceeding pair of data must be masked.

**TIMING DIAGRAM - 14: READ WITH AUTO-PRECHARGE
(EXAMPLE @ CL = 2, BL = 4, Multiple Bank Operation)**



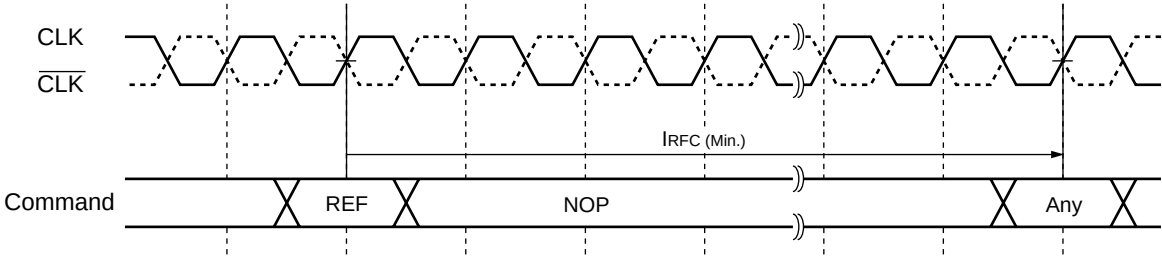
Note: Back to back Read with Auto-precharge (READA) command to the different bank in active state is possible. However, any new command to the same bank applied READA command can only be issued after $(BL/2) \times t_{CK} + I_{RP}$.

**TIMING DIAGRAM - 15: WRITE WITH AUTO-PRECHARGE
(EXAMPLE @ CL = 2, BL = 4, Multiple Bank Operation)**

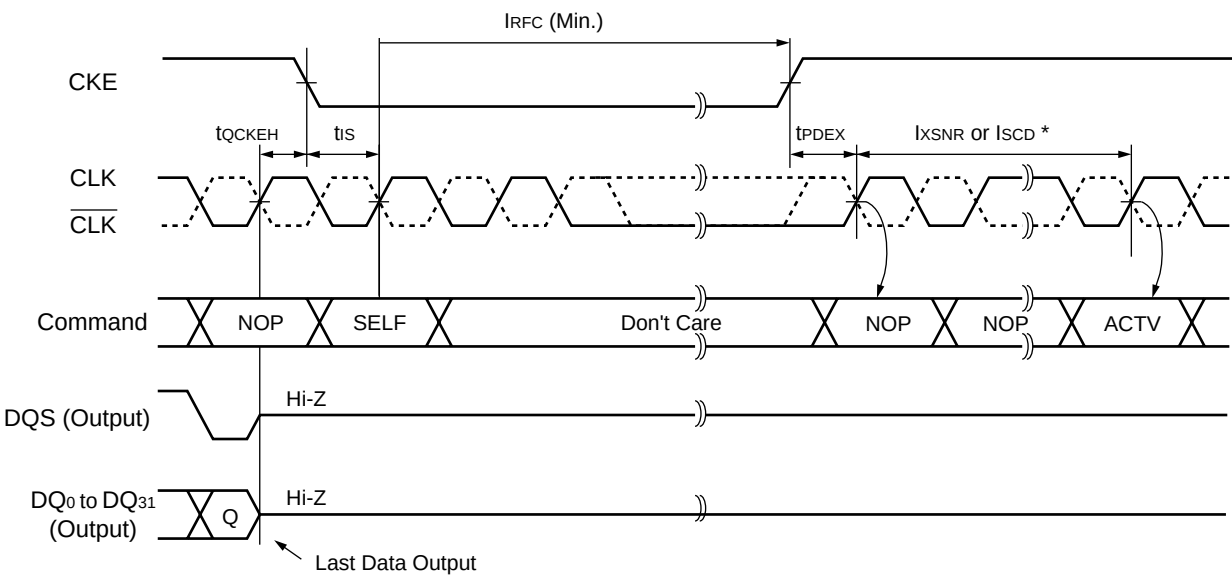


Note: Back to back Write with Auto-precharge (WRITA) command to the different bank in active state is possible. However, any new command to the same bank applied WRITA command can only be issued after I_{WAL} .

TIMING DIAGRAM - 16: AUTO-REFRESH ENTRY AND EXIT

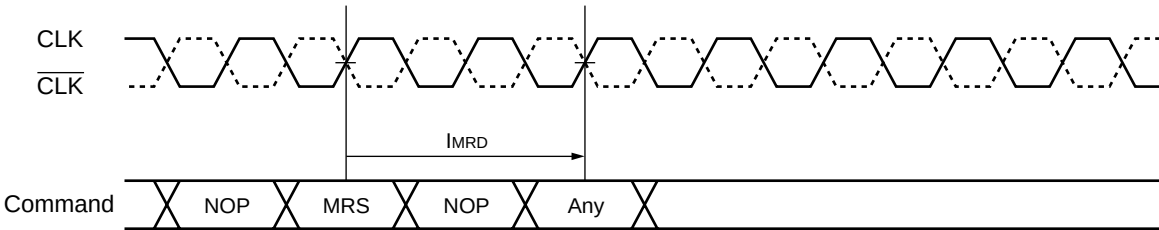


TIMING DIAGRAM - 17: SELF-REFRESH ENTRY AND EXIT



Note * :CKE must maintain High level and stable clock must be provided during the I_{SCD} period.
After Self-refresh exit, I_{xSNR} must be satisfied for at least specified period before any command (except for read) input.

TIMING DIAGRAM - 18: MODE REGISTER SET

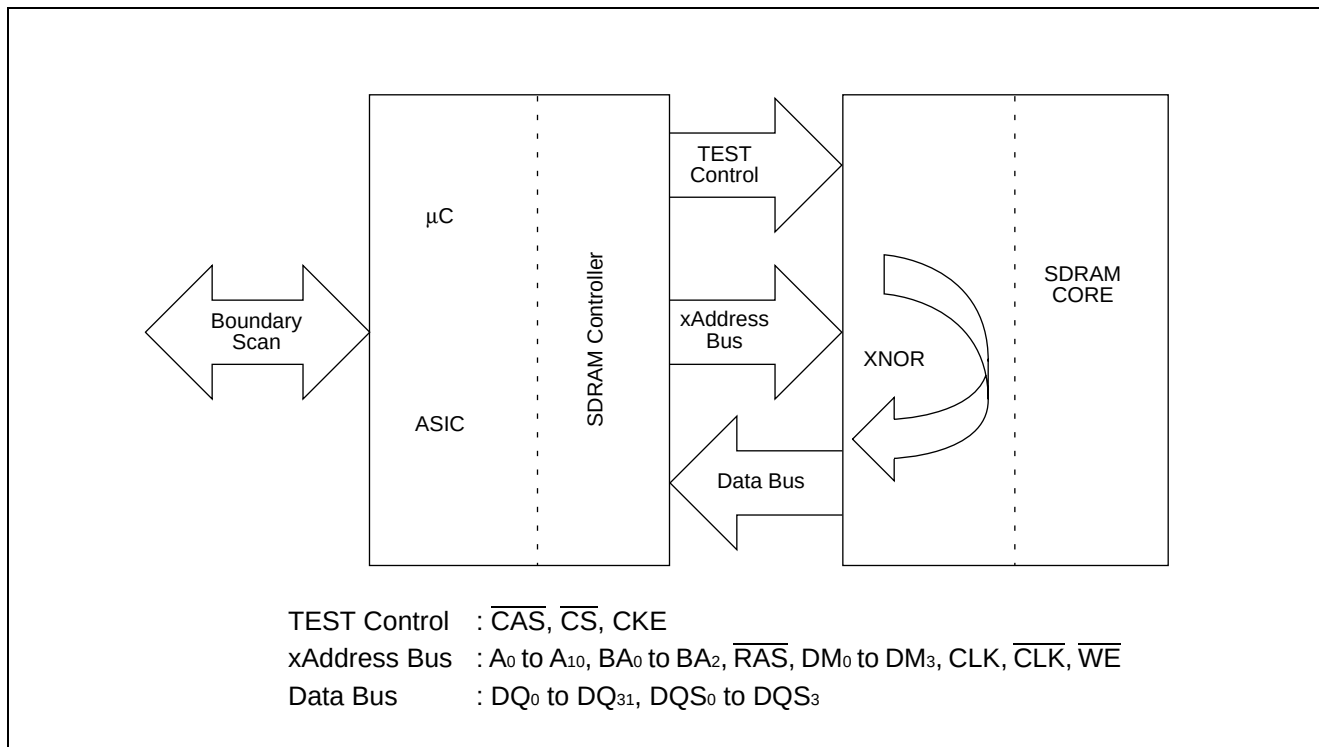


Note: MRS command must be issued after the last data is appeared on each DQ.

■ SCITT TEST MODE

ABOUT SCITT

SCITT (Static Component Interconnection Test Technology) is an XNOR circuit based test technology that is used for testing interconnection between SDRAM and SDRAM controller on the printed circuit boards. SCITT provides inexpensive board level test mode in combination with boundary-scan. The basic idea is simple, consider all output of SDRAM as output of XNOR circuit and each output pin has a unique mapping on the input of SDRAM. The ideal schematic block diagram is as shown below.



It is static and provides easy test pattern that result in a high diagnostic resolution for detecting all open/short faults.

SCITT TEST SEQUENCE

The followings are the SCITT test sequence. SCITT Test can be executed after power-on and prior to Precharge command in "■ FUNCTION DESCRIPTION POWER-UP INITIALIZATION". Once Precharge command is issued to SDRAM, it never get back to SCITT Test Mode during regular operation unless reset power supply for the purpose of a fail-safe way in get in and out of test mode.

1. Maintain all input signals (except CLK, $\overline{\text{CLK}}$) to be Low state (or at least CKE to be Low) and maintain CLK and $\overline{\text{CLK}}$ to be complementary state.
2. Apply V_{DD} voltage to all V_{DD} pins before or at the same time as V_{DDQ} pins.
3. Apply V_{DD} voltage to all V_{DDQ} pins before or at the same time as V_{REF} and V_{TT} .
4. Apply V_{REF} and V_{TT} (V_{TT} is applied to the system).
5. Maintain stable power for a minimum of 100 μ s.
6. Enter SCITT test mode.
7. Execute SCITT test.
8. Exit from SCITT mode.

It is required to follow Power On Sequence to execute read or write operation.

9. Start clock after all power supplies reached in a specified operating range and maintain stable condition for a minimum of 200 μ s.
10. After the minimum of 200 μ s stable power and clock, apply NOP condition and take CKE to be High state.
11. Issue Precharge All Banks (PALL) command or Precharge Single Bank (PRE) command to every banks.
12. Issue EMRS to enable DLL, DE = Low.
13. Issue Mode Register Set command (MRS) to reset DLL, DR = High. An additional clock input for I_{PCD} *¹ period is required to lock the DLL.
14. Apply minimum of two Auto-refresh command (REF).*²
15. Program the mode register by Mode Register Set command (MRS) with DR = Low.*²

The 6,7,8 steps define the SCITT mode available. It is possible to skip these steps if necessary (Refer to "■ FUNCTION DESCRIPTION POWER-UP INITIALIZATION").

Notes: *1. The I_{PCD} depends on operating clock period. The I_{PCD} is counted from "DLL Reset" at step-13 to any command input at step-15.

*2. The Mode Register Set command (MRS) can be issued before two Auto-refresh cycle.

MB81P643287-50/-60

COMMAND TRUTH TABLE Note *1

	Control			Input						Output	
	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	A ₀ to A ₁₀ , BA ₀ to BA ₂	DM ₀ to DM ₃	CLK	$\overline{\text{CLK}}$	DQ ₀ to DQ ₃₁	DQS ₀ to DQS ₃
SCITT mode entry	H→L *2	L	L	X	X	X	X	H	L	X	X
								L	H		
SCITT mode exit	L→H *3	H *5	L *5	X	X	X	X	X	X	X	X
SCITT mode output enable *4	L	L	H	V	V	V	V	V	V	V	V

Notes: *1. L = Logic Low, H = Logic High, V = Valid, X = either L or H

*2. The SCITT mode entry command assumes the first $\overline{\text{CAS}}$ falling edge with $\overline{\text{CS}} = \text{CKE} = \text{L}$ and CLK, $\overline{\text{CLK}}$ signals are complementary after power on.

*3. The SCITT mode exit command assumes the first $\overline{\text{CAS}}$ rising edge after the test mode entry.

*4. Refer the test code table.

*5. $\overline{\text{CS}} = \text{H}$ or CKE = L is necessary to disable outputs in SCITT mode exit.

TEST CODE TABLE

DQ₀ to DQ₃₁ and DQS₀ to DQS₃ output data is static and is determined by following logic during the SCITT mode operation.

$DQ_0 = \overline{RAS} \text{ xnor } A_0$	$DQ_{12} = \overline{RAS} \text{ xnor } BA_0$	$DQ_{24} = A_0 \text{ xnor } A_4$
$DQ_1 = \overline{RAS} \text{ xnor } A_1$	$DQ_{13} = \overline{RAS} \text{ xnor } BA_2$	$DQ_{25} = A_0 \text{ xnor } A_5$
$DQ_2 = \overline{RAS} \text{ xnor } A_2$	$DQ_{14} = \overline{RAS} \text{ xnor } DM_0$	$DQ_{26} = A_0 \text{ xnor } A_6$
$DQ_3 = \overline{RAS} \text{ xnor } A_3$	$DQ_{15} = \overline{RAS} \text{ xnor } DM_1$	$DQ_{27} = A_0 \text{ xnor } A_7$
$DQ_4 = \overline{RAS} \text{ xnor } A_4$	$DQ_{16} = \overline{RAS} \text{ xnor } DM_2$	$DQ_{28} = A_0 \text{ xnor } A_8$
$DQ_5 = \overline{RAS} \text{ xnor } A_5$	$DQ_{17} = \overline{RAS} \text{ xnor } DM_3$	$DQ_{29} = A_0 \text{ xnor } A_9$
$DQ_6 = \overline{RAS} \text{ xnor } A_6$	$DQ_{18} = \overline{RAS} \text{ xnor } CLK$	$DQ_{30} = A_0 \text{ xnor } A_{10}$
$DQ_7 = \overline{RAS} \text{ xnor } A_7$	$DQ_{19} = \overline{RAS} \text{ xnor } \overline{CLK}$	$DQ_{31} = A_0 \text{ xnor } BA_0$
$DQ_8 = \overline{RAS} \text{ xnor } A_8$	$DQ_{20} = \overline{RAS} \text{ xnor } \overline{WE}$	$DQS_0 = A_0 \text{ xnor } BA_1$
$DQ_9 = \overline{RAS} \text{ xnor } A_9$	$DQ_{21} = A_0 \text{ xnor } A_1$	$DQS_1 = A_0 \text{ xnor } BA_2$
$DQ_{10} = \overline{RAS} \text{ xnor } A_{10}$	$DQ_{22} = A_0 \text{ xnor } A_2$	$DQS_2 = A_0 \text{ xnor } DM_0$
$DQ_{11} = \overline{RAS} \text{ xnor } BA_1$	$DQ_{23} = A_0 \text{ xnor } A_3$	$DQS_3 = A_0 \text{ xnor } DM_1$

- EXAMPLE OF TEST CODE TABLE

Input bus																					Output bus																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																				
RAS	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	BA0	BA1	BA2	DM0	DM1	DM2	DM3	CLK	WE	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7	DQ8	DQ9	DQ10	DQ11	DQ12	DQ13	DQ14	DQ15	DQ16	DQ17	DQ18	DQ19	DQ20	DQ21	DQ22	DQ23	DQ24	DQ25	DQ26	DQ27	DQ28	DQ29	DQ30	DQ31	DQ32	DQ33	DQ34	DQ35	DQ36	DQ37	DQ38	DQ39	DQ40	DQ41	DQ42	DQ43	DQ44	DQ45	DQ46	DQ47	DQ48	DQ49	DQ50	DQ51	DQ52	DQ53	DQ54	DQ55	DQ56	DQ57	DQ58	DQ59	DQ60	DQ61	DQ62	DQ63	DQ64	DQ65	DQ66	DQ67	DQ68	DQ69	DQ70	DQ71	DQ72	DQ73	DQ74	DQ75	DQ76	DQ77	DQ78	DQ79	DQ80	DQ81	DQ82	DQ83	DQ84	DQ85	DQ86	DQ87	DQ88	DQ89	DQ90	DQ91	DQ92	DQ93	DQ94	DQ95	DQ96	DQ97	DQ98	DQ99	DQ100	DQ101	DQ102	DQ103	DQ104	DQ105	DQ106	DQ107	DQ108	DQ109	DQ110	DQ111	DQ112	DQ113	DQ114	DQ115	DQ116	DQ117	DQ118	DQ119	DQ120	DQ121	DQ122	DQ123	DQ124	DQ125	DQ126	DQ127	DQ128	DQ129	DQ130	DQ131	DQ132	DQ133	DQ134	DQ135	DQ136	DQ137	DQ138	DQ139	DQ140	DQ141	DQ142	DQ143	DQ144	DQ145	DQ146	DQ147	DQ148	DQ149	DQ150	DQ151	DQ152	DQ153	DQ154	DQ155	DQ156	DQ157	DQ158	DQ159	DQ160	DQ161	DQ162	DQ163	DQ164	DQ165	DQ166	DQ167	DQ168	DQ169	DQ170	DQ171	DQ172	DQ173	DQ174	DQ175	DQ176	DQ177	DQ178	DQ179	DQ180	DQ181	DQ182	DQ183	DQ184	DQ185	DQ186	DQ187	DQ188	DQ189	DQ190	DQ191	DQ192	DQ193	DQ194	DQ195	DQ196	DQ197	DQ198	DQ199	DQ200	DQ201	DQ202	DQ203	DQ204	DQ205	DQ206	DQ207	DQ208	DQ209	DQ210	DQ211	DQ212	DQ213	DQ214	DQ215	DQ216	DQ217	DQ218	DQ219	DQ220	DQ221	DQ222	DQ223	DQ224	DQ225	DQ226	DQ227	DQ228	DQ229	DQ230	DQ231	DQ232	DQ233	DQ234	DQ235	DQ236	DQ237	DQ238	DQ239	DQ240	DQ241	DQ242	DQ243	DQ244	DQ245	DQ246	DQ247	DQ248	DQ249	DQ250	DQ251	DQ252	DQ253	DQ254	DQ255	DQ256	DQ257	DQ258	DQ259	DQ260	DQ261	DQ262	DQ263	DQ264	DQ265	DQ266	DQ267	DQ268	DQ269	DQ270	DQ271	DQ272	DQ273	DQ274	DQ275	DQ276	DQ277	DQ278	DQ279	DQ280	DQ281	DQ282	DQ283	DQ284	DQ285	DQ286	DQ287	DQ288	DQ289	DQ290	DQ291	DQ292	DQ293	DQ294	DQ295	DQ296	DQ297	DQ298	DQ299	DQ300	DQ301	DQ302	DQ303	DQ304	DQ305	DQ306	DQ307	DQ308	DQ309	DQ310	DQ311	DQ312	DQ313	DQ314	DQ315	DQ316	DQ317	DQ318	DQ319	DQ320	DQ321	DQ322	DQ323	DQ324	DQ325	DQ326	DQ327	DQ328	DQ329	DQ330	DQ331	DQ332	DQ333	DQ334	DQ335	DQ336	DQ337	DQ338	DQ339	DQ340	DQ341	DQ342	DQ343	DQ344	DQ345	DQ346	DQ347	DQ348	DQ349	DQ350	DQ351	DQ352	DQ353	DQ354	DQ355	DQ356	DQ357	DQ358	DQ359	DQ360	DQ361	DQ362	DQ363	DQ364	DQ365	DQ366	DQ367	DQ368	DQ369	DQ370	DQ371	DQ372	DQ373	DQ374	DQ375	DQ376	DQ377	DQ378	DQ379	DQ380	DQ381	DQ382	DQ383	DQ384	DQ385	DQ386	DQ387	DQ388	DQ389	DQ390	DQ391	DQ392	DQ393	DQ394	DQ395	DQ396	DQ397	DQ398	DQ399	DQ400	DQ401	DQ402	DQ403	DQ404	DQ405	DQ406	DQ407	DQ408	DQ409	DQ410	DQ411	DQ412	DQ413	DQ414	DQ415	DQ416	DQ417	DQ418	DQ419	DQ420	DQ421	DQ422	DQ423	DQ424	DQ425	DQ426	DQ427	DQ428	DQ429	DQ430	DQ431	DQ432	DQ433	DQ434	DQ435	DQ436	DQ437	DQ438	DQ439	DQ440	DQ441	DQ442	DQ443	DQ444	DQ445	DQ446	DQ447	DQ448	DQ449	DQ450	DQ451	DQ452	DQ453	DQ454	DQ455	DQ456	DQ457	DQ458	DQ459	DQ460	DQ461	DQ462	DQ463	DQ464	DQ465	DQ466	DQ467	DQ468	DQ469	DQ470	DQ471	DQ472	DQ473	DQ474	DQ475	DQ476	DQ477	DQ478	DQ479	DQ480	DQ481	DQ482	DQ483	DQ484	DQ485	DQ486	DQ487	DQ488	DQ489	DQ490	DQ491	DQ492	DQ493	DQ494	DQ495	DQ496	DQ497	DQ498	DQ499	DQ500	DQ501	DQ502	DQ503	DQ504	DQ505	DQ506	DQ507	DQ508	DQ509	DQ510	DQ511	DQ512	DQ513	DQ514	DQ515	DQ516	DQ517	DQ518	DQ519	DQ520	DQ521	DQ522	DQ523	DQ524	DQ525	DQ526	DQ527	DQ528	DQ529	DQ530	DQ531	DQ532	DQ533	DQ534	DQ535	DQ536	DQ537	DQ538	DQ539	DQ540	DQ541	DQ542	DQ543	DQ544	DQ545	DQ546	DQ547	DQ548	DQ549	DQ550	DQ551	DQ552	DQ553	DQ554	DQ555	DQ556	DQ557	DQ558	DQ559	DQ560	DQ561	DQ562	DQ563	DQ564	DQ565	DQ566	DQ567	DQ568	DQ569	DQ570	DQ571	DQ572	DQ573	DQ574	DQ575	DQ576	DQ577	DQ578	DQ579	DQ580	DQ581	DQ582	DQ583	DQ584	DQ585	DQ586	DQ587	DQ588	DQ589	DQ590	DQ591	DQ592	DQ593	DQ594	DQ595	DQ596	DQ597	DQ598	DQ599	DQ600	DQ601	DQ602	DQ603	DQ604	DQ605	DQ606	DQ607	DQ608	DQ609	DQ610	DQ611	DQ612	DQ613	DQ614	DQ615	DQ616	DQ617	DQ618	DQ619	DQ620	DQ621	DQ622	DQ623	DQ624	DQ625	DQ626	DQ627	DQ628	DQ629	DQ630	DQ631	DQ632	DQ633	DQ634	DQ635	DQ636	DQ637	DQ638	DQ639	DQ640	DQ641	DQ642	DQ643	DQ644	DQ645	DQ646	DQ647	DQ648	DQ649	DQ650	DQ651	DQ652	DQ653	DQ654	DQ655	DQ656	DQ657	DQ658	DQ659	DQ660	DQ661	DQ662	DQ663	DQ664	DQ665	DQ666	DQ667	DQ668	DQ669	DQ670	DQ671	DQ672	DQ673	DQ674	DQ675	DQ676	DQ677	DQ678	DQ679	DQ680	DQ681	DQ682	DQ683	DQ684	DQ685	DQ686	DQ687	DQ688	DQ689	DQ690	DQ691	DQ692	DQ693	DQ694	DQ695	DQ696	DQ697	DQ698	DQ699	DQ700	DQ701	DQ702	DQ703	DQ704	DQ705	DQ706	DQ707	DQ708	DQ709	DQ710	DQ711	DQ712	DQ713	DQ714	DQ715	DQ716	DQ717	DQ718	DQ719	DQ720	DQ721	DQ722	DQ723	DQ724	DQ725	DQ726	DQ727	DQ728	DQ729	DQ730	DQ731	DQ732	DQ733	DQ734	DQ735	DQ736	DQ737	DQ738	DQ739	DQ740	DQ741	DQ742	DQ743	DQ744	DQ745	DQ746	DQ747	DQ748	DQ749	DQ750	DQ751	DQ752	DQ753	DQ754	DQ755	DQ756	DQ757	DQ758	DQ759	DQ760	DQ761	DQ762	DQ763	DQ764	DQ765	DQ766	DQ767	DQ768	DQ769	DQ770	DQ771	DQ772	DQ773	DQ774	DQ775	DQ776	DQ777	DQ778	DQ779	DQ780	DQ781	DQ782	DQ783	DQ784	DQ785	DQ786	DQ787	DQ788	DQ789	DQ790	DQ791	DQ792	DQ793	DQ794	DQ795	DQ796	DQ797	DQ798	DQ799	DQ800	DQ801	DQ802	DQ803	DQ804	DQ805	DQ806	DQ807	DQ808	DQ809	DQ810	DQ811	DQ812	DQ813	DQ814	DQ815	DQ816	DQ817	DQ818	DQ819	DQ820	DQ821	DQ822	DQ823	DQ824	DQ825	DQ826	DQ827	DQ828	DQ829	DQ830	DQ831	DQ832	DQ833	DQ834	DQ835	DQ836	DQ837	DQ838	DQ839	DQ840	DQ841	DQ842	DQ843	DQ844	DQ845	DQ846	DQ847	DQ848	DQ849	DQ850	DQ851	DQ852	DQ853	DQ854	DQ855	DQ856	DQ857	DQ858	DQ859	DQ860	DQ861	DQ862	DQ863	DQ864	DQ865	DQ866	DQ867	DQ868	DQ869	DQ870	DQ871	DQ872	DQ873	DQ874	DQ875	DQ876	DQ877	DQ878	DQ879	DQ880	DQ881	DQ882	DQ883	DQ884	DQ885	DQ886	DQ887	DQ888	DQ889	DQ890	DQ891	DQ892	DQ893	DQ894	DQ895	DQ896	DQ897	DQ898	DQ899	DQ900	DQ901	DQ902	DQ903	DQ904	DQ905	DQ906	DQ907	DQ908	DQ909	DQ910	DQ911	DQ912	DQ913	DQ914	DQ915	DQ916	DQ917	DQ918	DQ919	DQ920	DQ921	DQ922	DQ923	DQ924	DQ925	DQ926	DQ927	DQ928	DQ929	DQ930	DQ931	DQ932	DQ933	DQ934	DQ935	DQ936	DQ937	DQ938	DQ939	DQ940	DQ941	DQ942	DQ943	DQ944	DQ945	DQ946	DQ947	DQ948	DQ949	DQ950	DQ951	DQ952	DQ953	DQ954	DQ955	DQ956	DQ957	DQ958	DQ959	DQ960	DQ961	DQ962	DQ963	DQ964	DQ965	DQ966	DQ967	DQ968	DQ969	DQ970	DQ971	DQ972	DQ973	DQ974	DQ975	DQ976	DQ977	DQ978	DQ979	DQ980	DQ981	DQ982	DQ983	DQ984	DQ985	DQ986	DQ987	DQ988	DQ989	DQ990	DQ991	DQ992	DQ993	DQ994	DQ995	DQ996	DQ997	DQ998	DQ999	DQ1000	DQ1001	DQ1002	DQ1003	DQ1004	DQ1005	DQ1006	DQ1007	DQ1008	DQ1009	DQ1010	DQ1011	DQ1012	DQ1013	DQ1014	DQ1015	DQ1016	DQ1017	DQ1018	DQ1019	DQ1020	DQ1021	DQ1022	DQ1023	DQ1024	DQ1025	DQ1026	DQ1027	DQ1028	DQ1029	DQ1030	DQ1031	DQ1032	DQ1033	DQ1034	DQ1035	DQ1036	DQ1037	DQ1038	DQ1039	DQ1040	DQ1041	DQ1042	DQ1043	DQ1044	DQ1045	DQ1046	DQ1047	DQ1048	DQ1049	DQ1050	DQ1051	DQ1052	DQ1053	DQ1054	DQ1055	DQ1056	DQ1057	DQ1058	DQ1059	DQ1060	DQ1061	DQ1062	DQ1063	DQ1064	DQ1065	DQ1066	DQ1067	DQ1068	DQ1069	DQ1070	DQ1071	DQ1072	DQ1073	DQ1074	DQ1075	DQ1076	DQ1077	DQ1078	DQ1079	DQ1080	DQ1081	DQ1082	DQ1083	DQ1084	DQ1085	DQ1086	DQ1087	DQ1088	DQ1089	DQ1090	DQ1091	DQ1092	DQ1093	DQ1094	DQ1095	DQ1096	DQ1097	DQ1098	DQ1099	DQ1100	DQ1101	DQ1102	DQ1103	DQ1104	DQ1105	DQ1106	DQ1107	DQ1108	DQ1109	DQ1110	DQ1111	DQ1112	DQ1113	DQ1114	DQ1115	DQ1116	DQ1117	DQ1118	DQ1119	DQ1120	DQ1121	DQ1122	DQ1123	DQ1124	DQ1125	DQ1126	DQ1127	DQ1128	DQ1129	DQ1130	DQ1131	DQ1132	DQ1133	DQ1134	DQ1135	DQ1136	DQ1137	DQ1138	DQ1139	DQ1140	DQ1141	DQ1142	DQ1143	DQ1144	DQ1145	DQ1146	DQ1147	DQ1148	DQ1149	DQ1150	DQ1151	DQ1152	DQ1153	DQ1154	DQ1155	DQ1156	DQ1157	DQ1158	DQ1159	DQ1160	DQ1161	DQ1162	DQ1163	DQ1164	DQ1165	DQ1166	DQ1167	DQ1168	DQ1169	DQ1170	DQ1171	DQ1172	DQ1173	DQ1174	DQ1175	DQ1176	DQ1177	DQ1178	DQ1179	DQ1180	DQ1181	DQ1182	DQ1183	DQ1184	DQ1185	DQ1186	DQ1187	DQ1188	DQ1189	DQ1190	DQ1191	DQ1192	DQ1193	DQ1194	DQ1195	DQ1196	DQ1197	DQ1198	DQ1199	DQ1200	DQ1201	DQ1202	DQ1203	DQ1204	DQ1205	DQ1206	DQ1207	DQ1208	DQ1209	DQ1210	DQ1211	DQ1212	DQ1213	DQ1214	DQ1215	DQ1216	DQ1217	DQ1218	DQ1219	DQ1220	DQ1221	DQ1222	DQ1223	DQ1224	DQ1225	DQ1226	DQ1227	DQ1228	DQ1229	DQ1230	DQ1231	DQ1232	DQ1233	DQ1234	DQ1235	DQ1236	DQ1237	DQ1238	DQ1239	DQ1240	DQ1241	DQ1242	DQ1243	DQ1244	DQ1245	DQ1246	DQ1247	DQ1248	DQ1249	DQ1250	DQ1251	DQ1252	DQ1253	DQ1254	DQ1255	DQ1256	DQ1257	DQ1258	DQ1259	DQ1260	DQ1261	DQ1262	DQ1263	DQ1264	DQ1265	DQ1266	DQ1267	DQ1268	DQ1269	DQ1270	DQ1271	DQ1272	DQ1273	DQ1274	DQ1275	DQ1276	DQ1277	DQ1278	DQ1279	DQ1280	DQ1281	DQ1282	DQ1283	DQ1284	DQ1285	DQ1286	DQ1287	DQ1288	DQ1289	DQ1290	DQ1291	DQ1292	DQ1293	DQ1294	DQ1295	DQ1296	DQ1297	DQ1298	DQ1299	DQ1300	DQ1301	DQ1302	DQ1303	DQ1304	DQ1305	DQ1306	DQ1307	DQ1308	DQ1309	DQ1310	DQ1311	DQ1312	DQ1313	DQ1314	DQ1315	DQ1316	DQ1317	DQ1318	DQ1319	DQ1320	DQ1321	DQ1322	DQ1323	DQ1324	DQ1325	DQ1326	DQ1327	DQ1328	DQ1329	DQ1330	DQ1331	DQ1332

0 = input Low, 1 = input High, L = output Low, H = output High

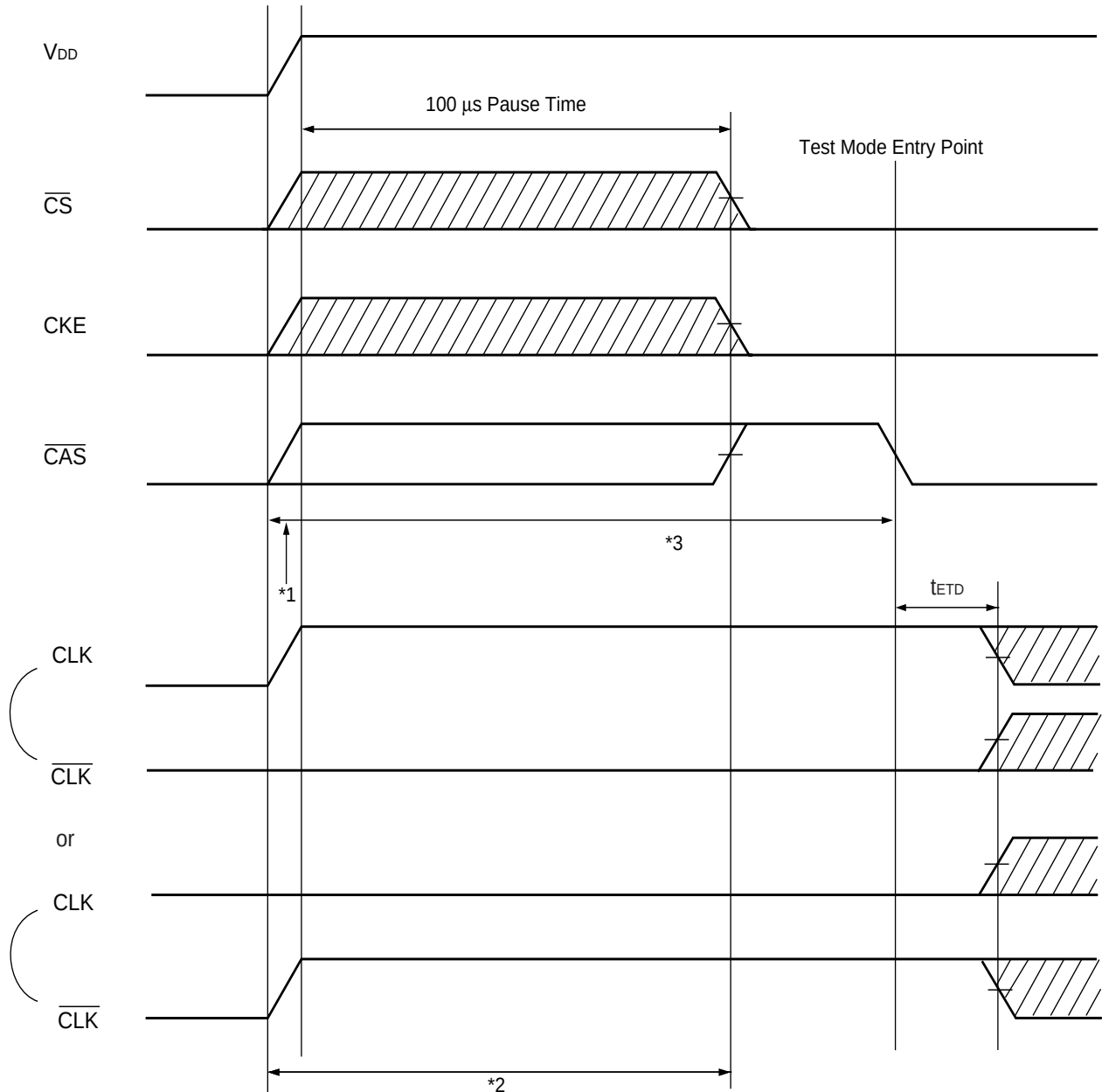
MB81P643287-50/-60

AC SPECIFICATION

Parameter	Description	Min.	Max.	Units
t_{TS}	Test mode entry set up time	10	—	ns
t_{TH}	Test mode entry hold time	10	—	ns
t_{EPD}	Test mode exit to power on sequence delay time	10	—	ns
t_{TLZ}	$\overline{CS}$, CKE to output in Low-Z time	0	—	ns
t_{THZ}	$\overline{CS}$, CKE to output in High-Z time	0	20	ns
t_{TCA}	Test mode access time from control signals (clock enable & chip select)	—	40	ns
t_{TIA}	Test mode Input access time	—	20	ns
t_{TOH}	Test mode Output Hold time	0	—	ns
t_{ETD}	Test mode entry to test delay time	10	—	ns
t_{TIH}	Test mode input hold time	30	—	ns

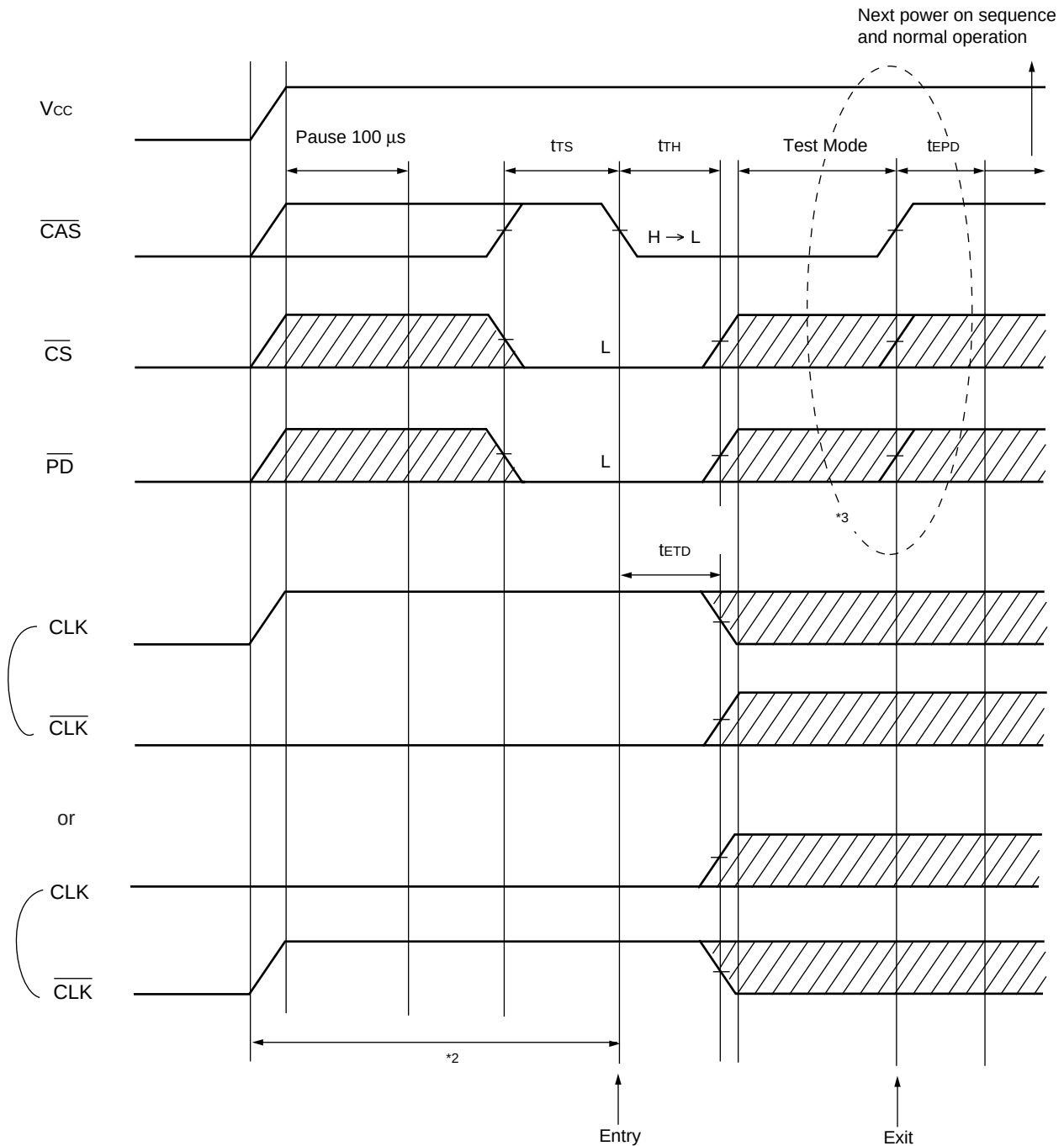
TIMING DIAGRAMS

TIMING DIAGRAM - 1: POWER-UP TIMING DIAGRAM



- Notes:
- *1. $\overline{CAS}$ shall be staid either High or Low at power on.
 - *2. All output buffers maintains in High-Z state regardless of the state of control signals except for $\overline{CAS}$ as long as the above timing is maintained.
 - *3. $\overline{CAS}$ must not be brought from High to Low.

TIMING DIAGRAM - 2 : SCITT TEST ENTRY AND EXIT *1

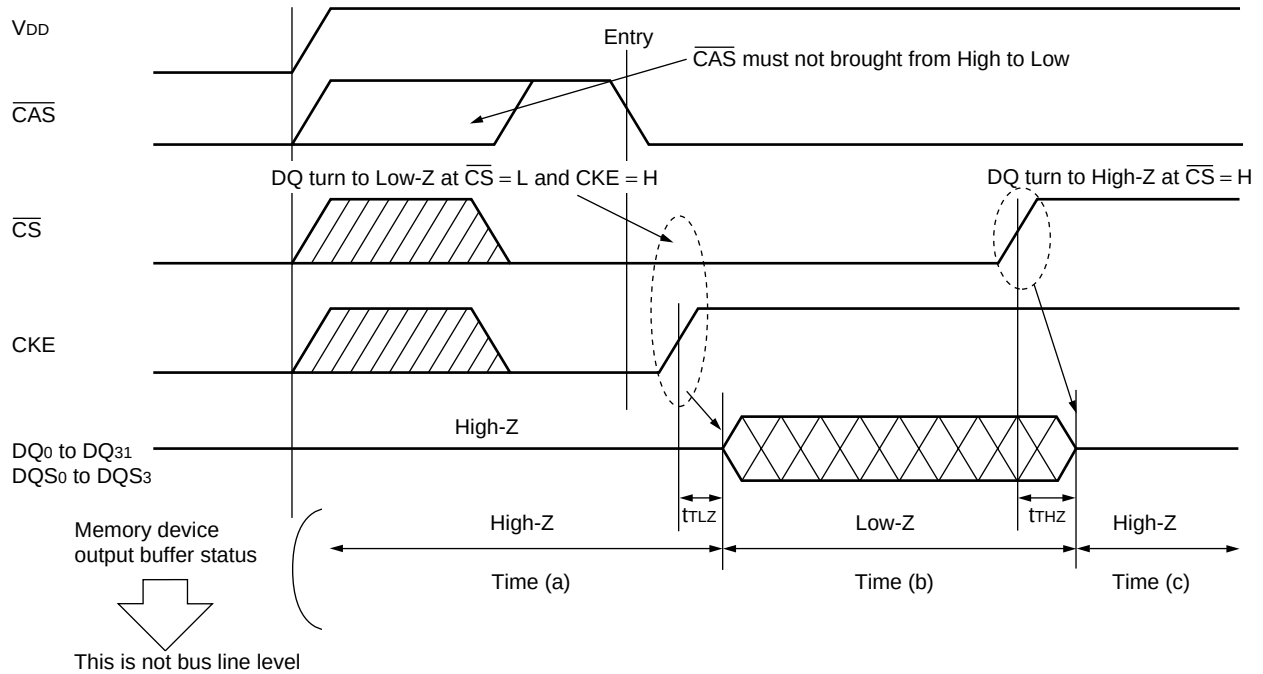


Notes: *1. If entry and exit operation have not been done correctly, $\overline{CAS}$, $\overline{CS}$, $\overline{CKE}$ pins will have some problems.

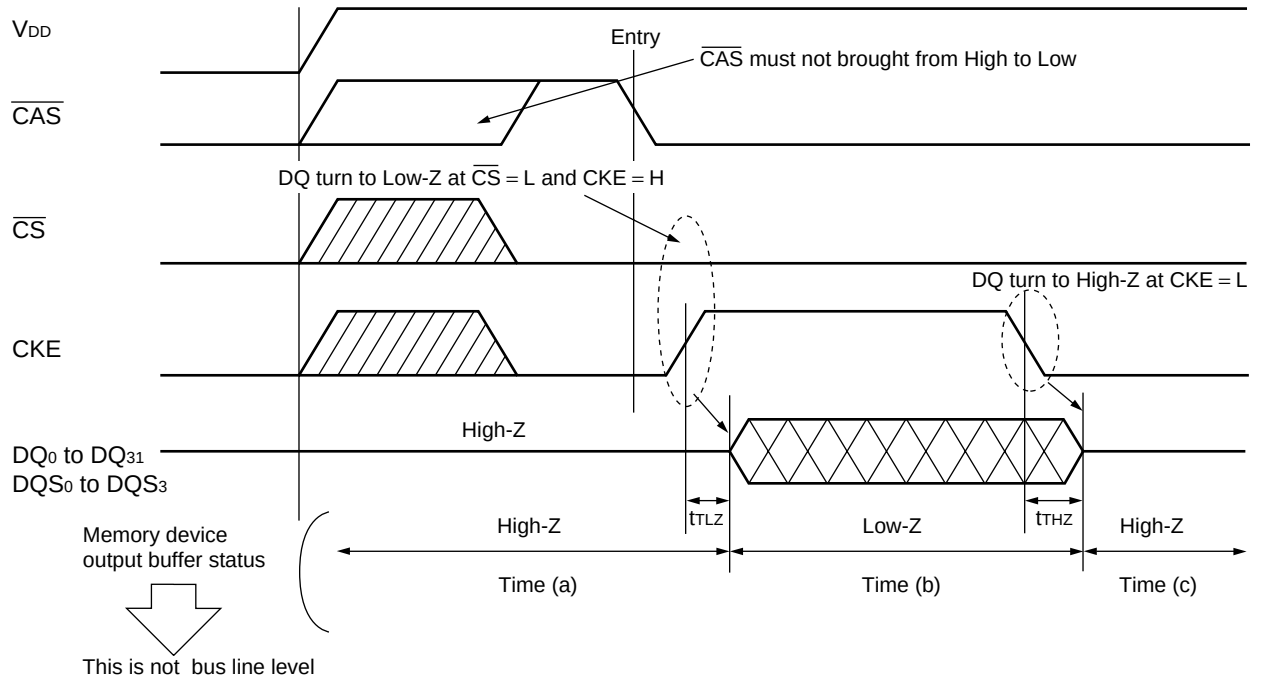
*2. PRE or PALL commands must not be asserted. Test mode is disable by those commands.

*3. Outputs must be disabled by $\overline{CS} = H$ or $CKE = L$ before Exit.

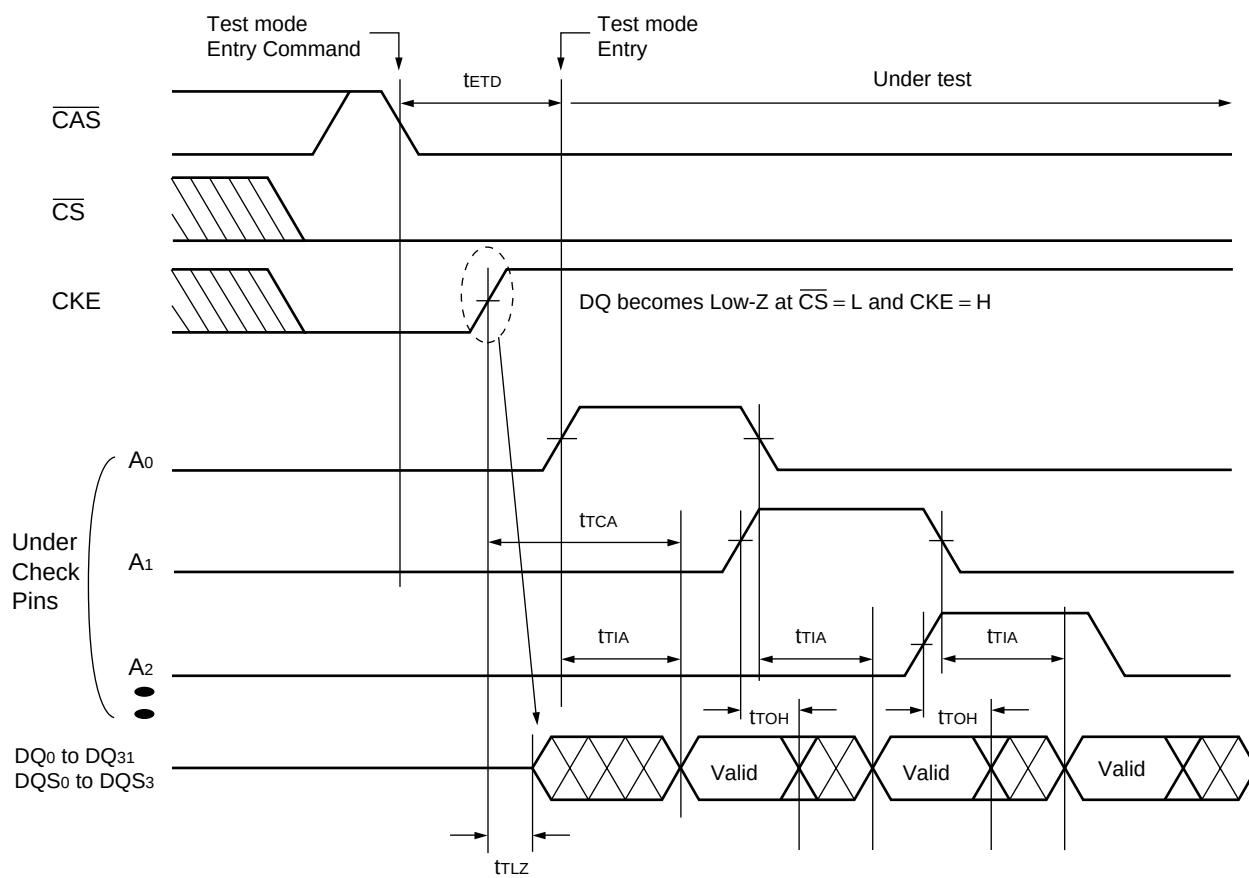
TIMING DIAGRAM - 3: OUTPUT CONTROL (1)



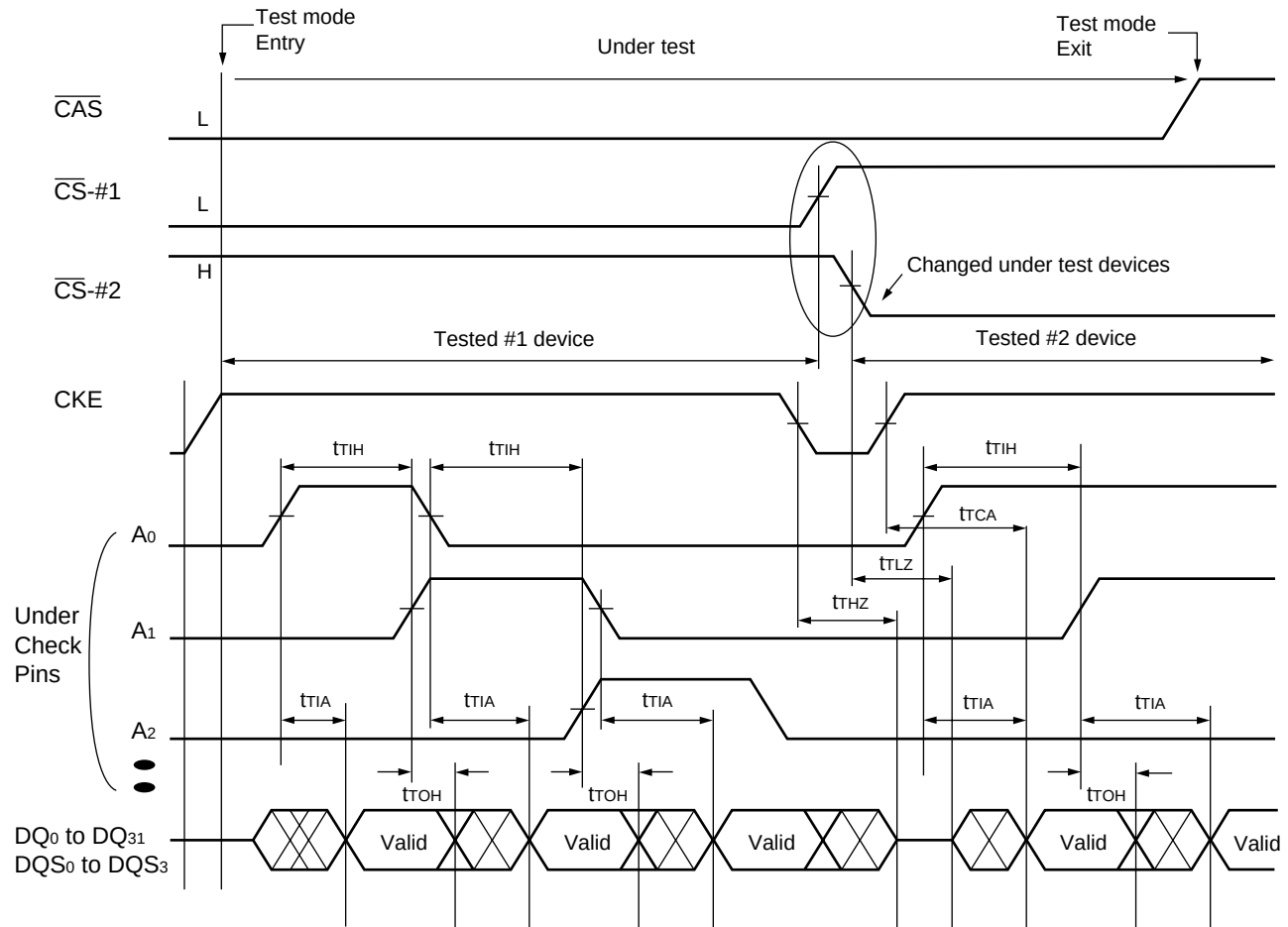
TIMING DIAGRAM - 4: OUTPUT CONTROL (2)



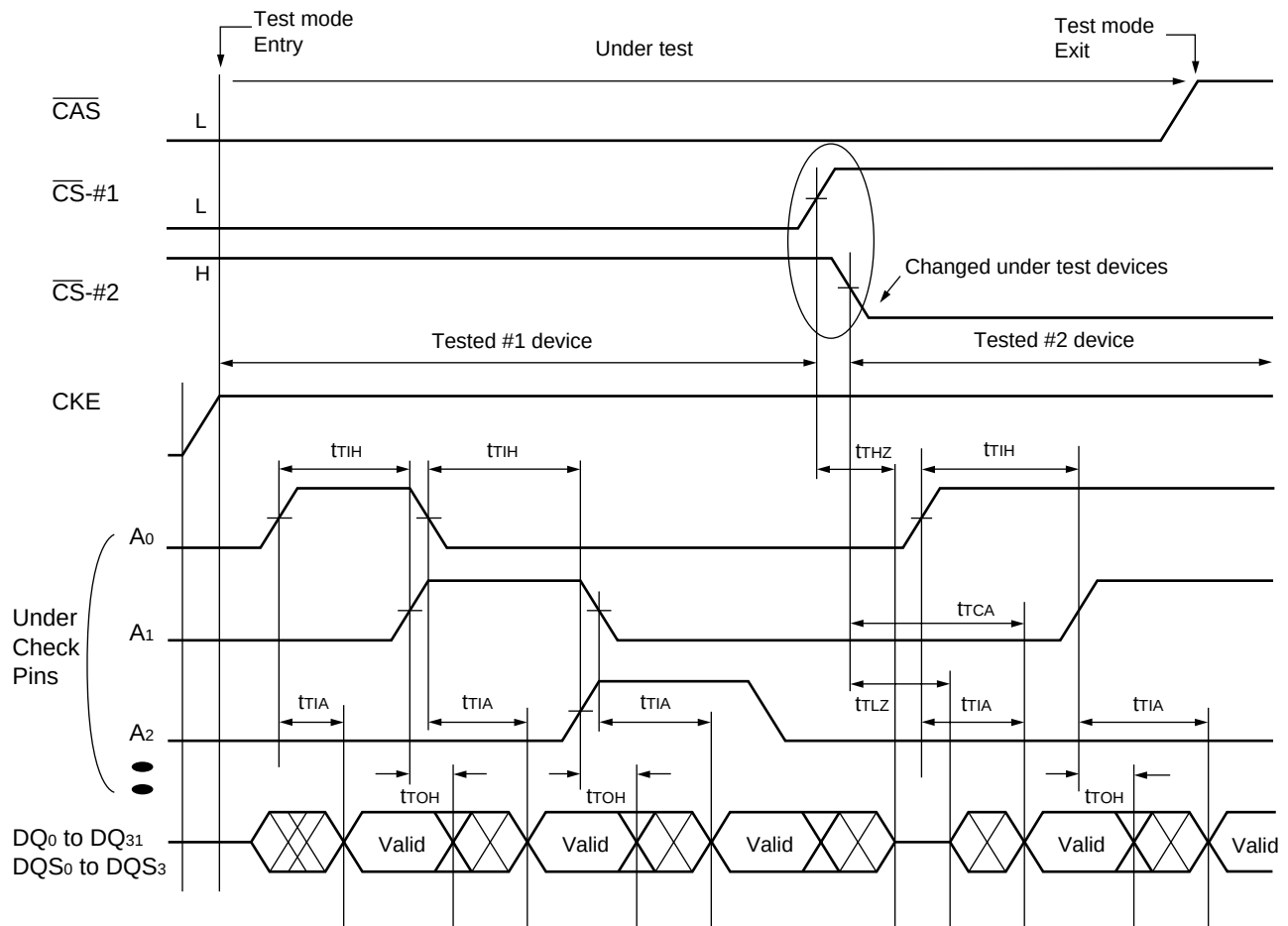
TIMING DIAGRAM - 5: TEST TIMING (1)



TIMING DIAGRAM - 6: TEST TIMING (2)



TIMING DIAGRAM - 7: TEST TIMING (3)



■ ORDERING INFORMATION

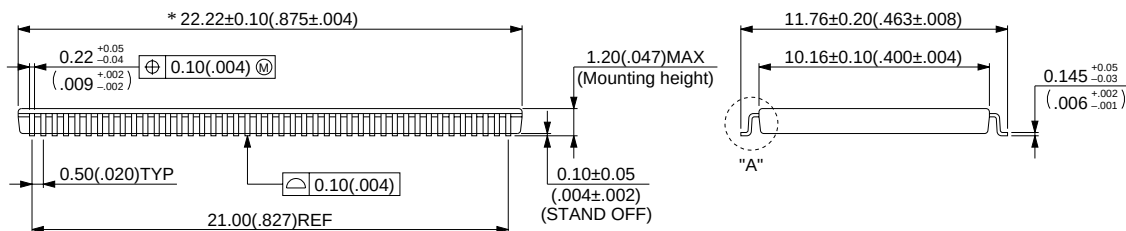
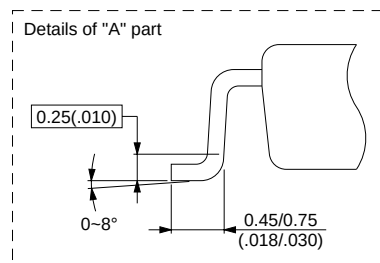
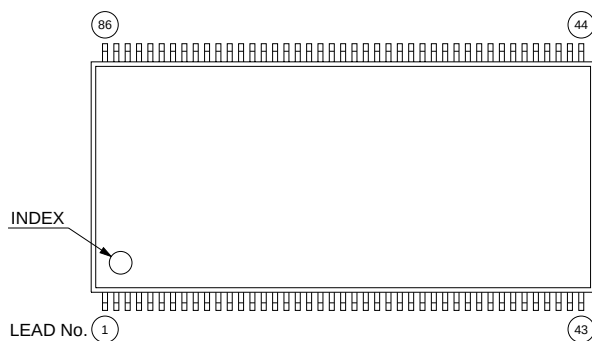
Part number	Package	Remarks
MB81P643287-50FN	86-pin plastic TSOP(II) (FPT-86P-M01)	—
MB81P643287-60FN		

MB81P643287-50/-60

■ PACKAGE DIMENSIONS

86-pin plastic TSOP (II)
(FPT-86P-M01)

*: Resin protrusion.(Each side: 0.15 (.006) Max.)



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Dimensions in mm (inches).

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